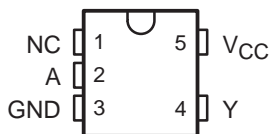


# SN74AHC1G04 SINGLE INVERTER GATE

SCLS3180 – MARCH 1996 – REVISED MARCH 2004

- Operating Range of 2 V to 5.5 V
- Max  $t_{pd}$  of 6.5 ns at 5 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 8$ -mA Output Drive at 5 V
- Schmitt Trigger Action at All Inputs Makes the Circuit Tolerant for Slower Input Rise and Fall Time
- Latch-Up Performance Exceeds 250 mA Per JESD 17

DBV OR DCK PACKAGES  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The SN74AHC1G04 contains one inverter gate. The device performs the Boolean function  $Y = \bar{A}$ .

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOT (SOT-23) – DBV	Reel of 3000	SN74AHC1G04DBVR	A04_
		Reel of 250	SN74AHC1G04DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74AHC1G04DCKR	AC_
		Reel of 250	SN74AHC1G04DCKT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

‡ The actual top-side marking has one additional character that designates the assembly/test site.

## FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

## logic diagram (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
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# SN74AHC1G04

## SINGLE INVERTER GATE

SCLS3180 – MARCH 1996 – REVISED MARCH 2004

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 3$ V	2.1	
		$V_{CC} = 5.5$ V	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 3$ V	0.9	
		$V_{CC} = 5.5$ V	1.65	
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	-50	μA
		$V_{CC} = 3.3$ V ± 0.3 V	-4	mA
		$V_{CC} = 5$ V ± 0.5 V	-8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	μA
		$V_{CC} = 3.3$ V ± 0.3 V	4	mA
		$V_{CC} = 5$ V ± 0.5 V	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V	100	ns/V
		$V_{CC} = 5$ V ± 0.5 V	20	
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN74AHC1G04 SINGLE INVERTER GATE

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9	2		1.9	V	
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1	0.1	V	
		3 V			0.1	0.1		
		4.5 V			0.1	0.1		
	I <sub>OL</sub> = 4 mA	3 V			0.36	0.44		
	I <sub>OL</sub> = 8 mA	4.5 V			0.36	0.44		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V				±0.1	±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V				1	10	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF	5	7.1		1	8.5	ns
t <sub>PHL</sub>				5	7.1		1	8.5	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	7.5	10.6		1	12	ns
t <sub>PHL</sub>				7.5	10.6		1	12	

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF	3.8	5.5		1	6.5	ns
t <sub>PHL</sub>				3.8	5.5		1	6.5	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	5.3	7.5		1	8.5	ns
t <sub>PHL</sub>				5.3	7.5		1	8.5	

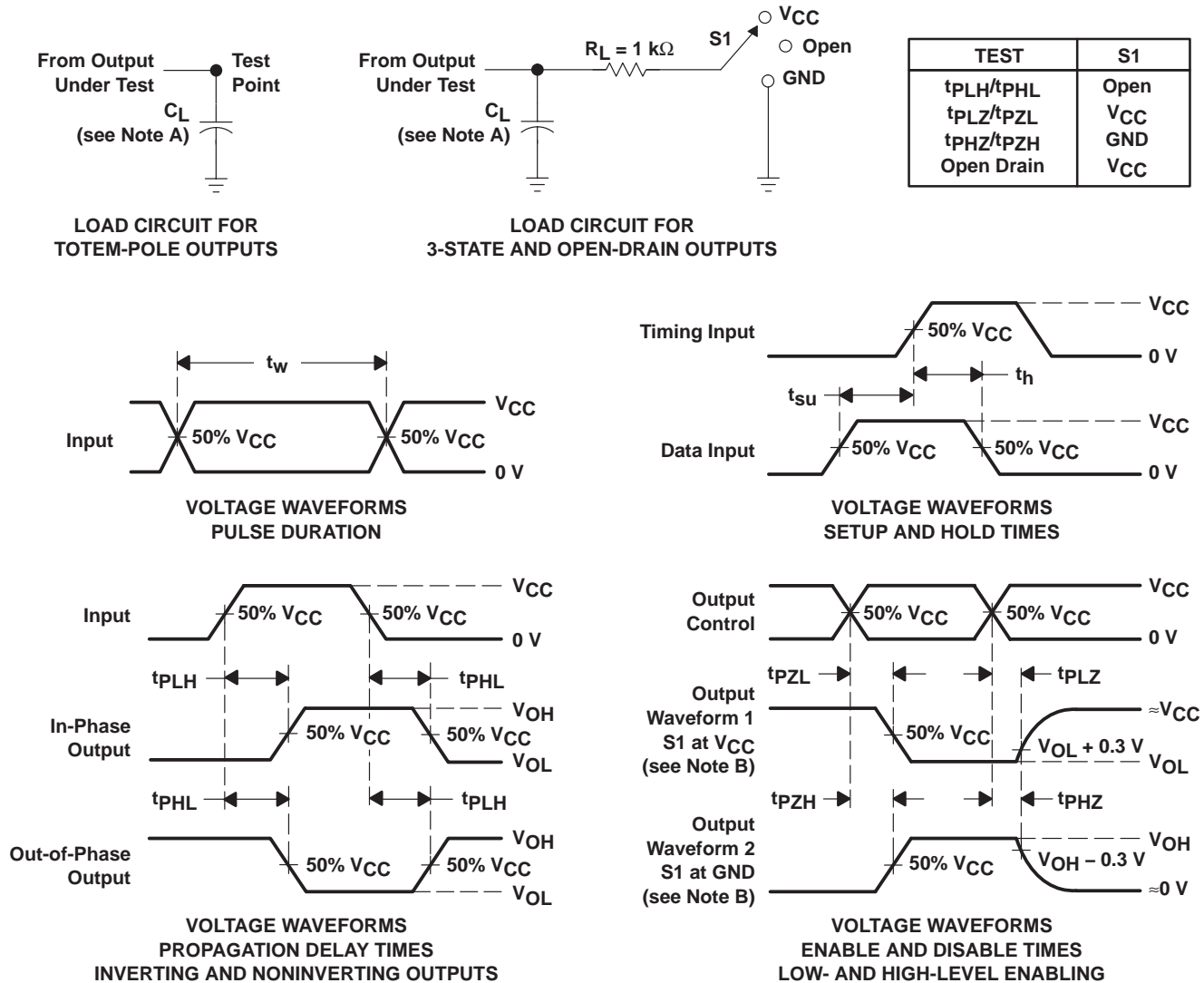
operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	No load, f = 1 MHz	12	pF

# SN74AHC1G04 SINGLE INVERTER GATE

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## PARAMETER MEASUREMENT INFORMATION

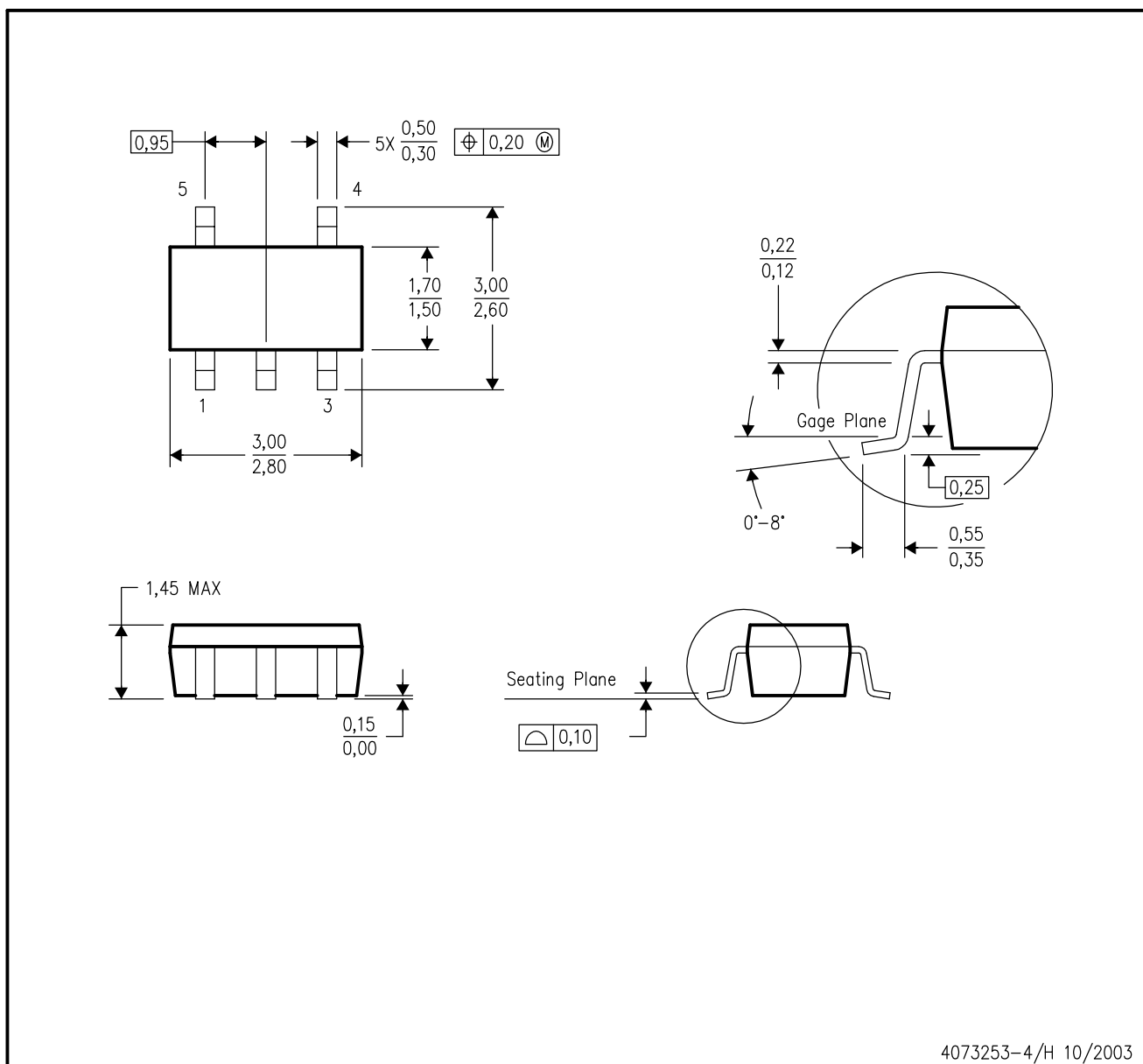


- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DBV (R-PDSO-G5)

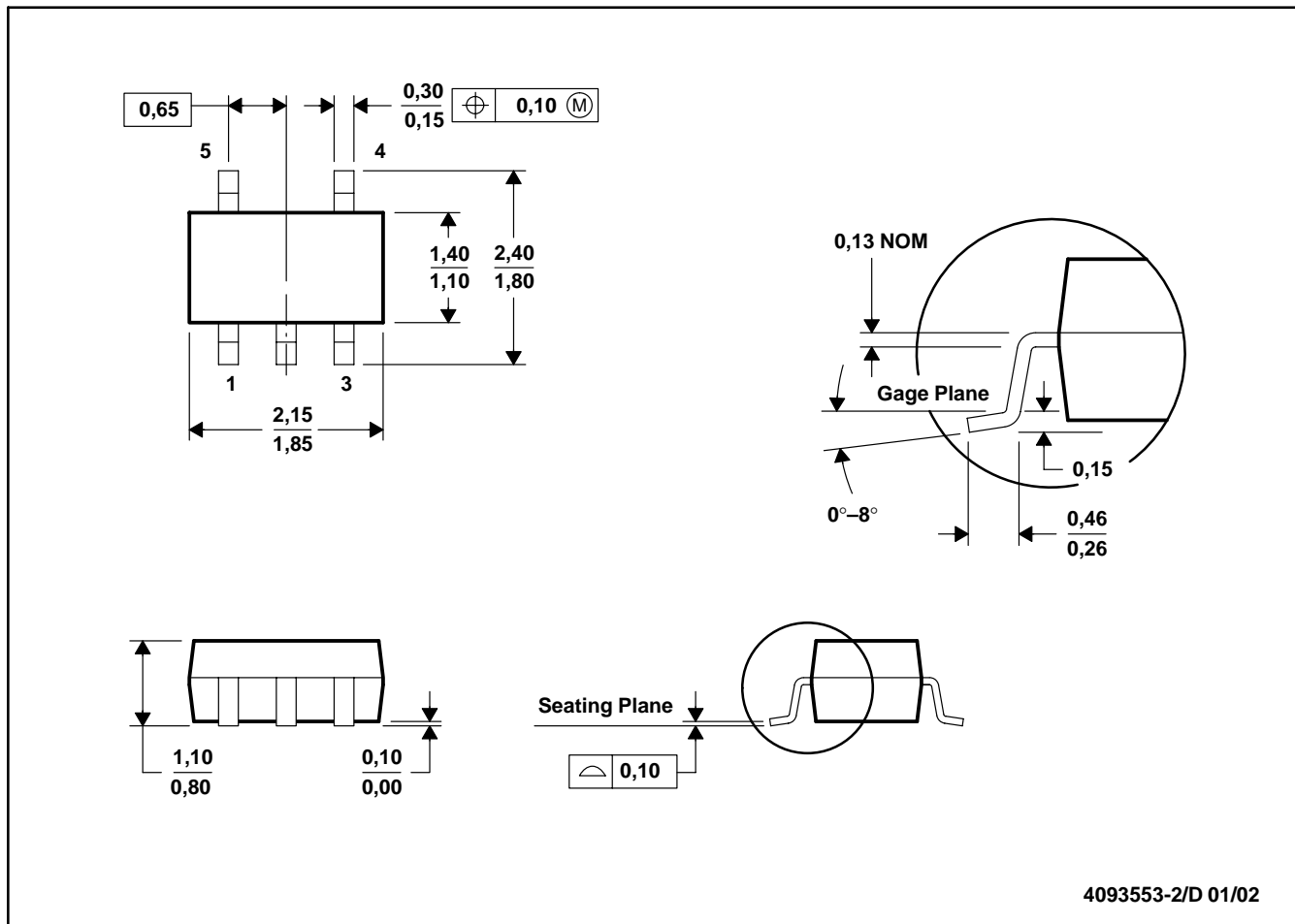
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.  
 D. Falls within JEDEC MO-178 Variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.  
 D. Falls within JEDEC MO-203

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