FAIRCHILD

SEMICONDUCTOR ™

74VHC138
3-to-8 Decoder/Demultiplexer

General Description

The VHC138 is an advanced high speed CMOS 3-to-8 decoder/demultiplexer fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

When the device is enabled, 3 binary select inputs (A_0, A_1 and A_2) determine which one of the outputs ($\overline{O}_0$–$\overline{O}_7$) will go LOW. When enable input E_3 is held LOW or either $\overline{E}_1$ or $\overline{E}_2$ is held HIGH, decoding function is inhibited and all outputs go HIGH. E_3, $\overline{E}_1$ and $\overline{E}_2$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems. An input protection circuit ensures that

0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

■ High Speed: t_{PD} = 5.7ns (typ) at T_A = 25°C

■ Low power dissipation: I_{CC} = 4 μA (max.) at T_A = 25°C

■ High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min.)

■ Power down protection provided on all inputs

■ Pin and function compatible with 74HC138

Ordering Code:

Order Number	Package Number	Package Description
74VHC138M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC138SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC138MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC138N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols

IEEE/IEC
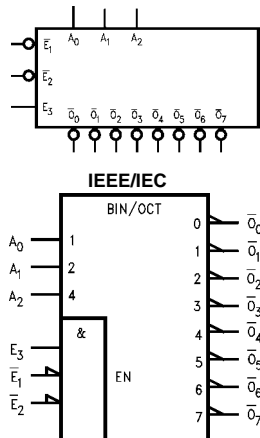
Connection Diagram
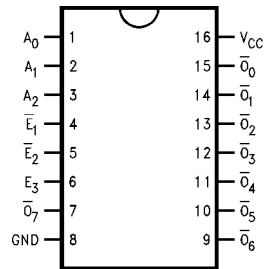
Pin Descriptions

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$–$\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$–$\overline{O}_7$	Outputs

Truth Table

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ± 0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ± 0.5V	0 ~ 20 ns/V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.
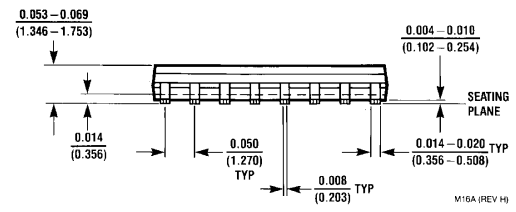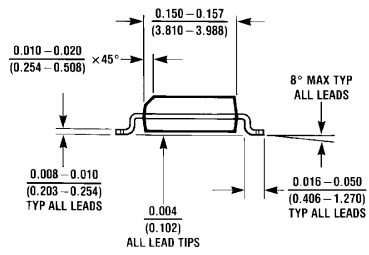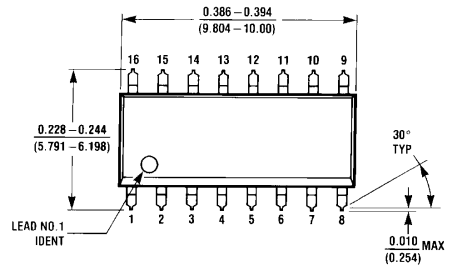
DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units	Conditions	
V_{IH}	HIGH Level Input Voltage	2.0	1.50			1.50		V		
		3.0 – 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Input Voltage	2.0			0.50		0.50	V		
		3.0 – 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 µA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 µA
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0 – 5.5			±0.1		±1.0	µA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	µA	V_{IN} = V_{CC} or GND	

74VHC138

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3 ± 0.3		8.2	11.4	1.0	13.5	ns	C_L = 15 pF
t_{PHL}	A_n to $\overline{O}_n$			10.0	15.8	1.0	18.0		C_L = 50 pF
		5.0 ± 0.5		5.7	8.1	1.0	9.5	ns	C_L = 15 pF
				7.2	10.1	1.0	11.5		C_L = 50 pF
t_{PLH}	Propagation Delay	3.3 ± 0.3		8.1	12.8	1.0	15.0	ns	C_L = 15 pF
t_{PHL}	E_3 to $\overline{O}_n$			10.6	16.3	1.0	18.5		C_L = 50 pF
		5.0 ± 0.5		5.6	8.1	1.0	9.5	ns	C_L = 15 pF
				7.1	10.1	1.0	11.5		C_L = 50 pF
t_{PLH}	Propagation Delay	3.3 ± 0.3		8.2	11.4	1.0	13.5	ns	C_L = 15 pF
t_{PHL}	$\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$			10.7	14.9	1.0	17.0		C_L = 50 pF
		5.0 ± 0.5		5.8	8.1	1.0	9.5	ns	C_L = 15 pF
				7.3	10.1	1.0	11.5		C_L = 50 pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance			34				pF	(Note 3)

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = $C_{PD} * V_{CC} * f_{IN} + I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted

0.386 − 0.394
(9.804 − 10.00)

16 15 14 13 12 11 10 9

0.228 − 0.244
(5.791 − 6.198)

30°
TYP

LEAD NO.1
IDENT

1   2   3   4   5   6   7   8

0.010 MAX
(0.254)

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008 TYP
(0.203)

0.014 − 0.020 TYP
(0.356 − 0.508)

M16A (REV H)

16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

16   9

0.295-0.319
(7.5-8.1)

0.205-0.213
(5.2-5.4)

1   8

0.394-0.402
(10.0-10.2)

(0.71)
(1.8)

0.006-0.010 TYP
(0.15-0.25)

0.006 (0.15)

SEATING
PLANE

0.050 TYP
(1.27)

0.067-0.083
(1.7-2.1)

0.000-0.010
(0-0.25)

0° - 8° TYP

0.014-0.020 TYP
(0.35-0.50)

(0.049 TYP)
(1.25)

0.016-0.031 TYP
(0.4-0.8)

M16D (REV B)
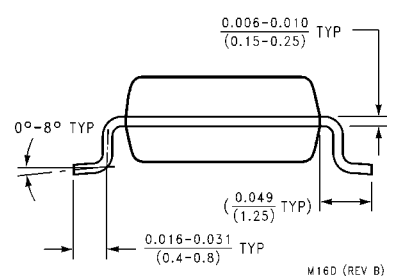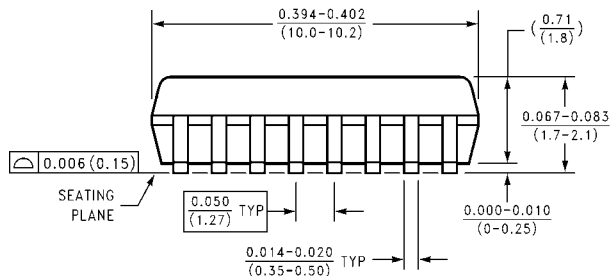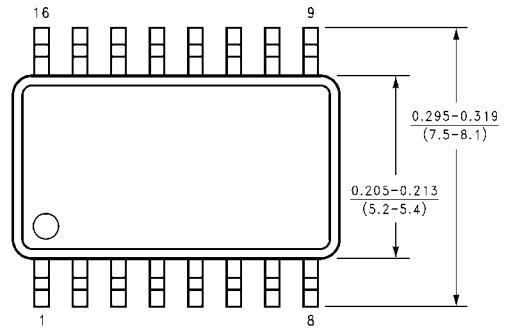
16-Lead Small Outline Package (SOP) EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS METRIC ONLY

7.72 TYP.
4.16 TYP.

(1.78 TYP)

0.42 TYP
0.65 TYP

LAND PATTERN RECOMMENDATION

5.0 ± 0.1
−A−
16   9

6.4

4.4 ± 0.1
−B−

3.2

1   8
PIN # 1 IDENT.

⌖ 0.2 C B A
ALL LEAD TIPS

GAGE PLANE
0.25

0°−8°
0.6 ± 0.1
SEATING PLANE

DETAIL A
TYPICAL, SCALE: 40X

⌖ 0.1 C
ALL LEAD TIPS

−C−

0.65 TYP

0.19 − 0.30 TYP

(0.90)

1.1 MAX TYP

0.10 ± 0.05 TYP

⊕ 0.13 Ⓜ A B Ⓢ C Ⓢ

SEE DETAIL A

0.09−0.20 TYP

MTC16 (REV C)
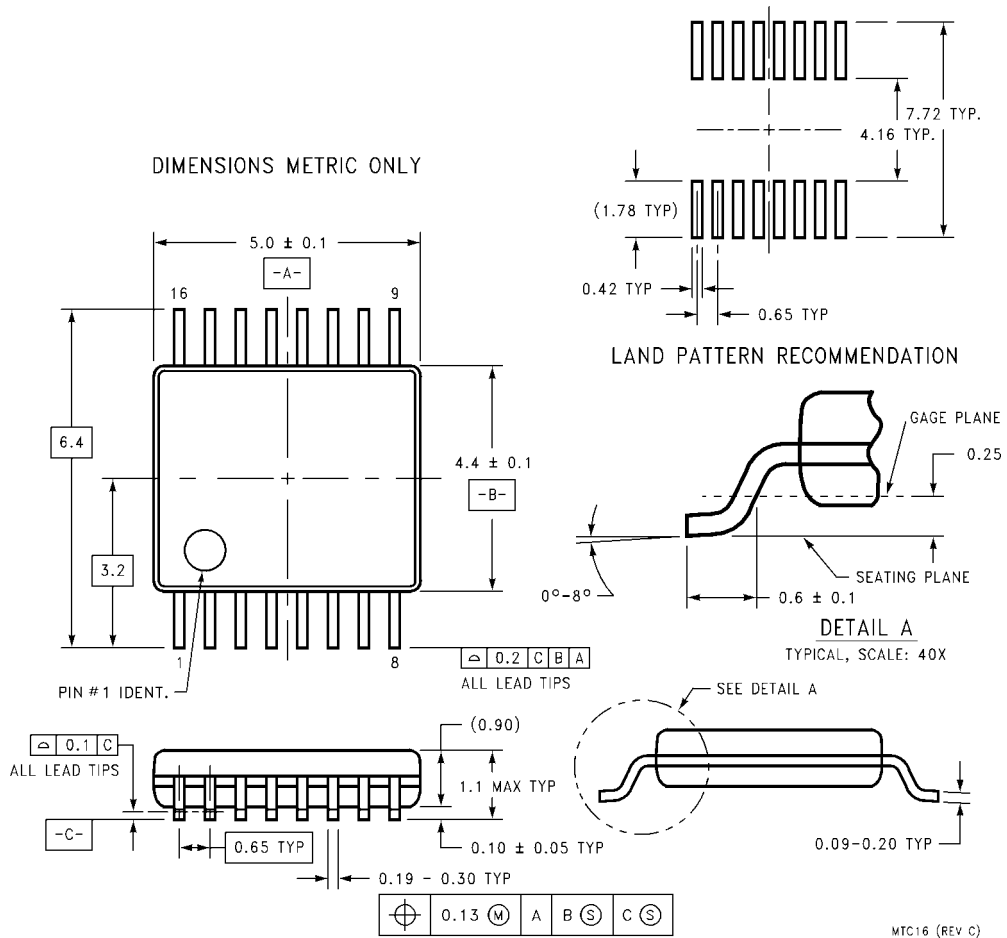
16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.740 – 0.780
(18.80 – 19.81)

0.090
(2.286)

16 15 14 13 12 11 10 9

0.250 ± 0.010
(6.350 ± 0.254)

PIN NO. 1
IDENT

1 2 3 4 5 6 7 8

OPTION 01

INDEX
AREA

16 15

PIN NO. 1
IDENT

1 2

OPTION 02

0.130 ± 0.005
(3.302 ± 0.127)

0.060
(1.524) TYP

4° TYP
OPTIONAL

0.065
(1.651)

0.300 – 0.320
(7.620 – 8.128)

0.145 – 0.200
(3.683 – 5.080)

0.020
(0.508) MIN

0.125 – 0.150
(3.175 – 3.810)

90° ± 4° TYP

0.030 ± 0.015
(0.762 ± 0.381)

95° ± 5°

0.008 – 0.016
(0.203 – 0.406) TYP

0.014 – 0.023
(0.356 – 0.584)
TYP

0.050 ± 0.010
(1.270 ± 0.254)
TYP

0.100 ± 0.010
(2.540 ± 0.254)
TYP

0.280
(7.112)
MIN

$(0.325 \genfrac{}{}{0pt}{}{+0.040}{-0.015})$

$(8.255 \genfrac{}{}{0pt}{}{+1.016}{-0.381})$

N16E (REV F)

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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