DS2003 High Current/Voltage Darlington Drivers

Check for Samples: DS2003

FEATURES

- **Seven High Gain Darlington Pairs**
- **High Output Voltage (V_{CE} = 50V)**
- **High Output Current (I_C = 350 mA)**
- **TTL, PMOS, CMOS Compatible**
- **Suppression Diodes for Inductive Loads**
- **Extended Temperature Range**

DESCRIPTION

The DS2003 comprises seven high voltage, high current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads and appropriate emitter base resistors for leakage.

The DS2003 has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5.0V.

The DS2003 offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

Connection Diagram

Top View

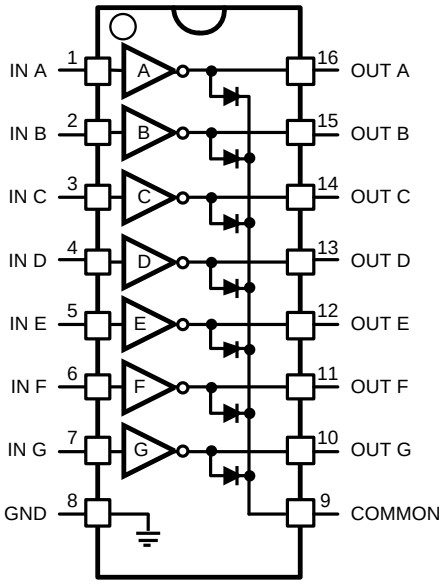

Figure 1.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Storage Temperature Range	−65°C to +150°C
Operating Temperature Range, T_A	
DS2003T	−40°C to +125°C
DS2003C	−40°C to +85°C
Junction Temperature Range, T_J	−40°C to +150°C
Lead Temperature	
Soldering, 10 seconds	265°C
ESD Ratings	
Human Body Model	+/-2000V
Machine Model	+/- 200V
Package Thermal Dissipation Ratings	
NFG0016E Package θ_{J-A}	88°C/W
D0016A Package θ_{J-A}	115°C/W
Input Voltage	−0.3V to 30V
Output Voltage	55V
Emitter-Base Voltage	6.0V
Continuous Collector Current	500 mA
Continuous Base Current	25 mA

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics provide conditions for actual device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

Electrical Characteristics

T_A = 25°C, unless otherwise specified (1)

Parameter		Test Conditions	Min	Typ	Max	Units
I_{CEX}	Output Leakage Current	T_A = 25°C, V_{CE} = 50V (Figure 6)			20	µA
		T_A = 85°C, V_{CE} = 50V (Figure 6)			100	
		T_A = 125°C, V_{CE} = 50V (Figure 6) for DS2003T			150	
$V_{CE(Sat)}$	Collector-Emitter Saturation Voltage	I_C = 350mA, I_B = 500µA (Figure 8)(2)		1.25	1.6	V
		I_C = 200mA, I_B = 350µA (Figure 8)		1.1	1.3	
		I_C = 100mA, I_B = 250µA (Figure 8)		0.9	1.1	
$I_{I(ON)}$	Input Current	V_I = 3.85V (Figure 9)		0.93	1.35	mA
$I_{I(OFF)}$	Input Current (3)	I_C = 500µA (Figure 10)	50	100		µA
		T_A = +25°C	50	100		
		T_A = +85°C	25	50		
		T_A = +125C for DS2003T	10	25		
$V_{I(ON)}$	Input Voltage (4)	V_{CE} = 2.0V, I_C = 200mA (Figure 11)			2.4	V
		V_{CE} = 2.0V, I_C = 250mA (Figure 11)			2.7	
		V_{CE} = 2.0V, I_C = 300mA (Figure 11)			3.0	
C_I	Input Capacitance			15	30	pF
t_{PLH}	Turn-On Delay	0.5 V_I to 0.5 V_O			1.0	µs
t_{PHL}	Turn-Off Delay	0.5 V_I to 0.5 V_O			1.0	µs

(1) All limits apply to the complete Darlington series except as specified for a single device type.
(2) Under normal operating conditions these units will sustain 350 mA per output with $V_{CE\ (Sat)}$ = 1.6V at 70°C with a pulse width of 20 ms and a duty cycle of 30%.
(3) The $I_{I(OFF)}$ current limit ensured against partial turn-on of the output.
(4) The $V_{I(ON)}$ voltage limit ensures a minimum output sink current per the specified test conditions.

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Electrical Characteristics (continued)

T_A = 25°C, unless otherwise specified (1)

Parameter		Test Conditions	Min	Typ	Max	Units
I_R	Clamp Diode Leakage Current	V_R = 50V (Figure 12)				µA
		T_A = 25°C		5	10	
		T_A = 85°C		10	50	
		T_A = 125°C for DS2003T		20	100	
V_F	Clamp Diode Forward Voltage	I_F = 350mA (Figure 13)		1.7	2.0	V

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Typical Performance Characteristics

Collector Current vs Saturation Voltage

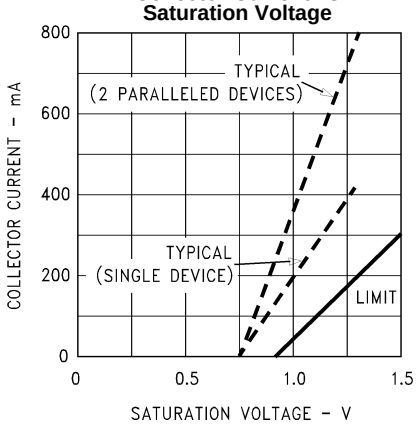

Figure 2.

Collector Current vs Input Current

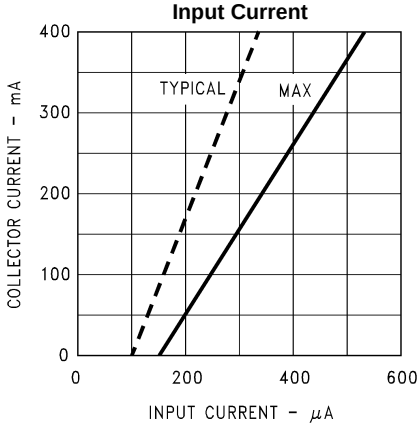

Figure 3.

Input Current vs Input Voltage

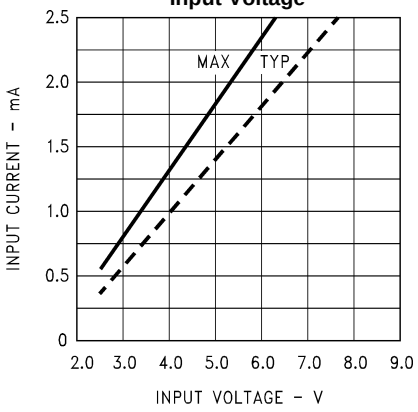

Figure 4.

Peak Collector Current vs Duty Cycle and Number of Outputs (N16E Package)

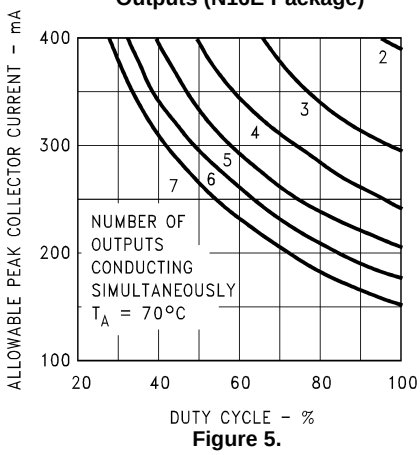

Figure 5.

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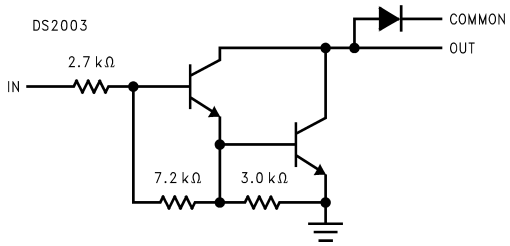
EQUIVALENT CIRCUITS



Test Circuits

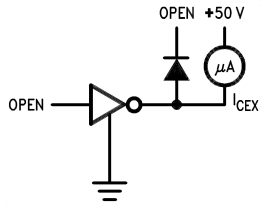


Figure 6.

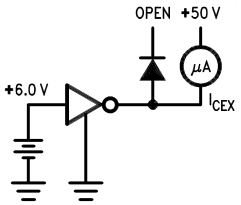


Figure 7.

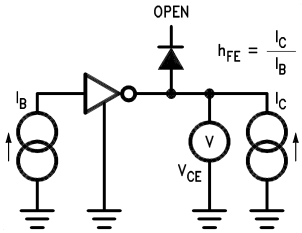


Figure 8.

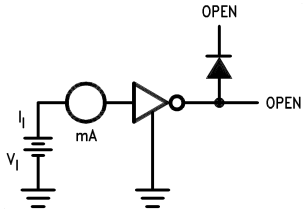


Figure 9.

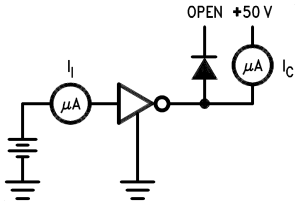


Figure 10.

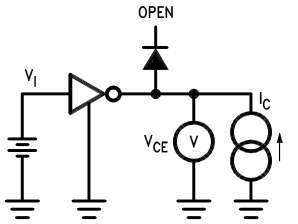


Figure 11.

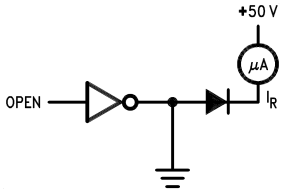


Figure 12.

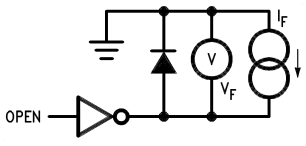


Figure 13.

Typical Applications

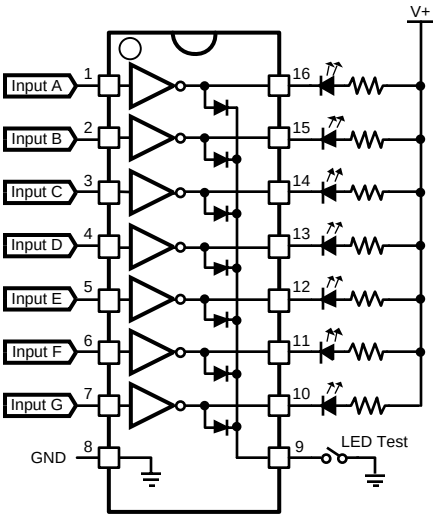


Figure 14. Typical LED Driver

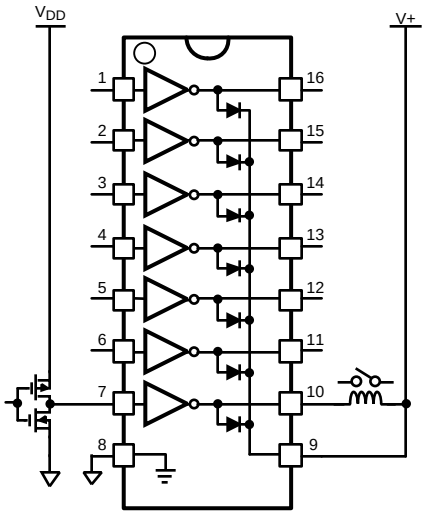


Figure 15. Typical Relay Driver

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REVISION HISTORY

Changes from Revision I (April 2013) to Revision J	Page
• Changed layout of National Data Sheet to TI format	6

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS2003CM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 125	DS2003CM	
DS2003CM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	DS2003CM	Samples
DS2003CMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN | Call TI	Level-1-260C-UNLIM	-40 to 125	DS2003CM	Samples
DS2003TM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 125	DS2003TM	
DS2003TM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	DS2003TM	Samples
DS2003TMX	NRND	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 125	DS2003TM	
DS2003TMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	DS2003TM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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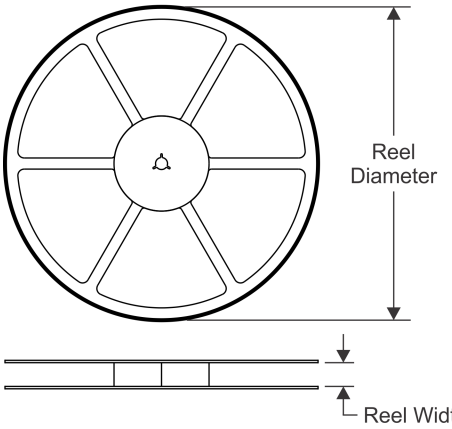
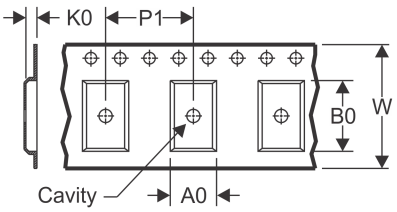
TAPE AND REEL INFORMATION

REEL DIMENSIONS

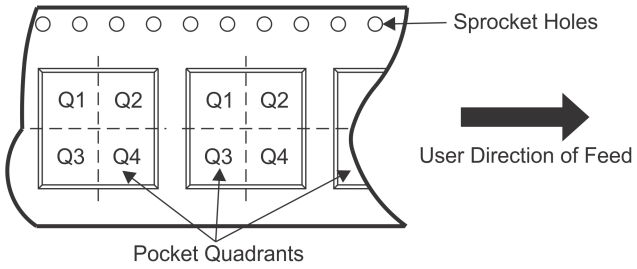


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

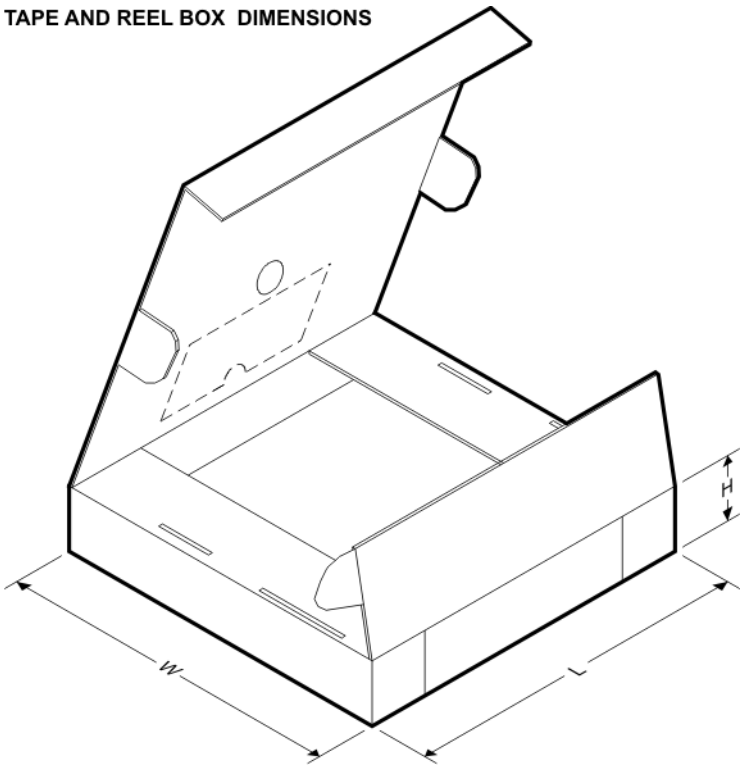
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS2003CMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS2003TMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS2003TMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

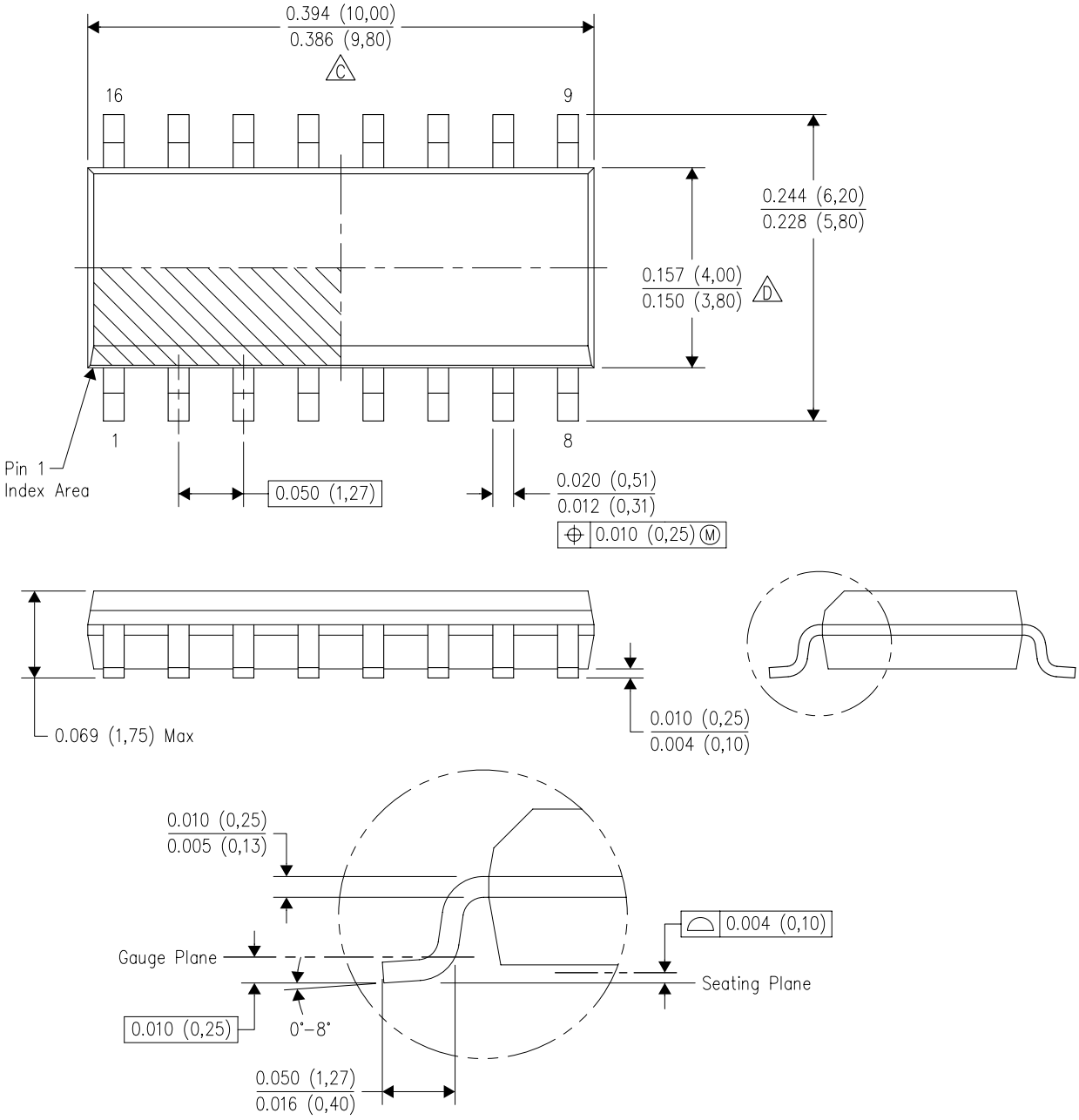
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS2003CMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0
DS2003TMX	SOIC	D	16	2500	367.0	367.0	35.0
DS2003TMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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