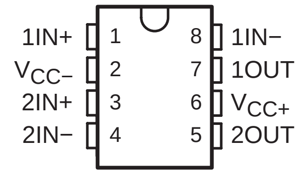
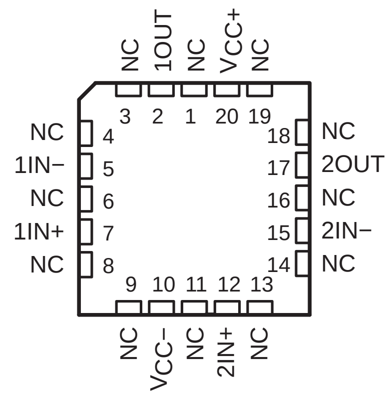
- **Single-Supply Operation**
  - **Input Voltage Range Extends to Ground**
  - **Output Swings to Ground While Sinking Current**
- **Input Offset Voltage**
  - **150 μV Max at 25°C for LT1013A**
- **Offset-Voltage Temperature Coefficient**
  - **2.5 μV/°C Max for LT1013A**
- **Input Offset Current**
  - **0.8 nA Max at 25°C for LT1013A**
- **High Gain . . . 1.5 V/μV Min (R_L = 2 kΩ), 0.8 V/μV Min (R_L = 600 kΩ) for LT1013A**
- **Low Supply Current . . . 0.5 mA Max at T_A = 25°C for LT1013A**
- **Low Peak-to-Peak Noise Voltage . . . 0.55 μV Typ**
- **Low Current Noise . . . 0.07 pA/$\sqrt{Hz}$ Typ**

LT1013, LT1013D . . . D PACKAGE
(TOP VIEW)

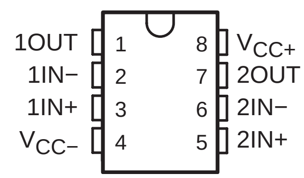


LT1013, LT1013A . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

LT1013, LT1013D . . . JG OR P PACKAGE
(TOP VIEW)



description/ordering information

The LT1013 devices are dual precision operational amplifiers, featuring high gain, low supply current, low noise, and low-offset-voltage temperature coefficient.

The LT1013 devices can be operated from a single 5-V power supply; the common-mode input voltage range includes ground, and the output can also swing to within a few millivolts of ground. Crossover distortion is eliminated. The LT1013 can be operated with both dual ±15-V and single 5-V supplies.

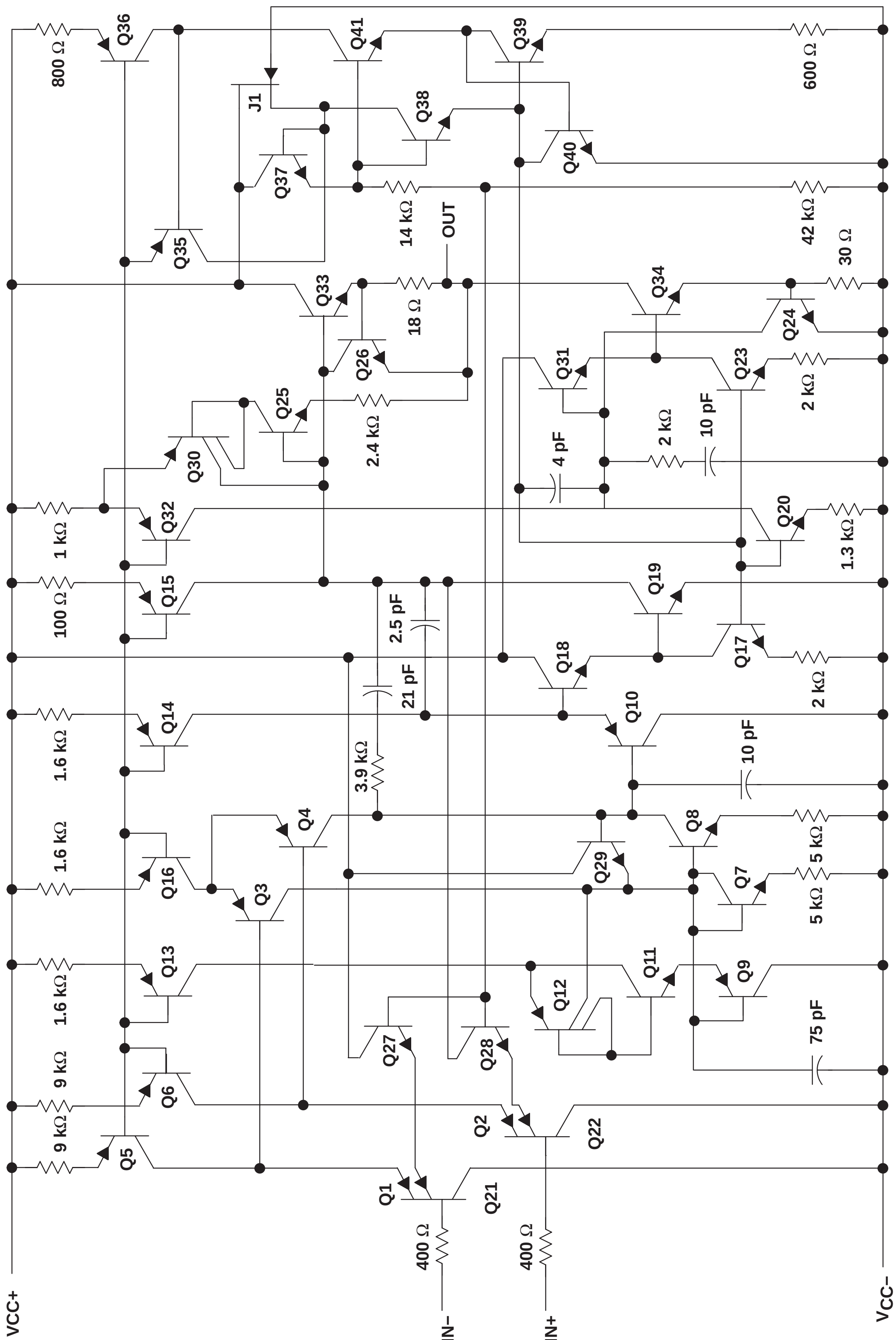
The LT1013C, LT1013AC, and LT1013D are characterized for operation from 0°C to 70°C. The LT1013I, LT1013AI, and LT1013DI are characterized for operation from −40°C to 105°C. The LT1013M, LT1013AM, and LT1013DM are characterized for operation over the full military temperature range of −55°C to 125°C.

ORDERING INFORMATION

T_A	V_{IO}max AT 25°C (μV)	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	300	P−DIP (P)	Tube of 50	LT1013CP	LT1013P
		SOIC (D)	Tube of 75	LT1013CD	1013C
			Reel of 2500	LT1013CDR	
	800	P−DIP (P)	Tube of 50	LT1013DP	LT1013DP
		SOIC (D)	Tube of 75	LT1013DD	1013D
			Reel of 2500	LT1013DDR	
−40°C to 105°C	800	P−DIP (P)	Tube of 50	LT1013DIP	LT1013DIP
		SOIC (D)	Tube of 75	LT1013DID	1013DI
			Reel of 2500	LT1013DIDR	
−55°C to 125°C	150	C−DIP (JG)	Tube of 50	LT1013AMJG	LT1013AMJG
		C−DIP (JGB)	Tube of 50	LT1013AMJGB	LT1013AMJGB
		LCCC (FK)	Tube of 55	LT1013AMFK	LT1013AMFK
		LCCC (FKB)	Tube of 55	LT1013AMFKB	LT1013AMFKB
	300	C−DIP (JG)	Tube of 50	LT1013MJG	LT1013MJG
		C−DIP (JGB)	Tube of 50	LT1013MJGB	LT1013MJGB
		LCCC (FKB)	Tube of 55	LT1013MFKB	LT1013MFKB
	800	SOIC (D)	Tube of 75	LT1013DMD	1013DM

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

schematic (each amplifier)



Component values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) †

Supply voltage (see Note 1): V_{CC+}	22 V
V_{CC-}	−22 V
Input voltage range, V_I (any input, see Note 1)	V_{CC-} − 5 V to V_{CC+}
Differential input voltage (see Note 2)	±30 V
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Package thermal impedance, θ_{JA} (see Notes 4 and 5): D package	97°C/W
P package	85°C/W
Operating virtual junction temperature, T_J	150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: JG package	300°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply.
4. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V, $V_{IC} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013C			LT1013AC			LT1013DC			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$	25°C		60	300		40	150		200	800	µV
			Full range			400			240			1000	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage		Full range		0.4	2.5		0.3	2		0.7	5	µV/°C
	Long-term drift of input offset voltage		25°C		0.5			0.4			0.5		µV/mo
I_{IO}	Input offset current		25°C		0.2	1.5		0.15	0.8		0.2	1.5	nA
			Full range			2.8			1.5			2.8	
I_{IB}	Input bias current		25°C		−15	−30		−12	−20		−15	−30	nA
			Full range			−38			−25			−38	
V_{ICR}	Common-mode input voltage range		25°C	−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		V
			Full range	−15 to 13			−15 to 13			−15 to 13			
V_{OM}	Maximum peak output voltage swing	$R_L = 2\ k\Omega$	25°C	±12.5	±14		±13	±14		±12.5	±14		V
			Full range	±12			±12.5			±12			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V, $R_L = 600\ \Omega$	25°C	0.5	0.2		0.8	2.5		0.5	2		V/µV
		$V_O = \pm10$ V, $R_L = 2\ k\Omega$	25°C	1.2	7		1.5	8		1.2	7		
			Full range	0.7			1			0.7			
CMRR	Common-mode rejection ratio	$V_{IC} = -15$ V to 13.5 V	25°C	97	114		100	117		97	114		dB
		$V_{IC} = -14.9$ V to 13 V	Full range	94			98			94			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC+} = \pm2$ V to ±18 V	25°C	100	117		103	120		100	117		dB
			Full range	97			101			97			
	Channel separation	$V_O = \pm10$ V, $R_L = 2\ k\Omega$	25°C	120	137		123	140		120	137		dB
r_{id}	Differential input resistance		25°C	70	300		100	400		70	300		MΩ
r_{ic}	Common-mode input resistance		25°C		4			5			4		GΩ
I_{CC}	Supply current per amplifier		25°C		0.35	0.55		0.35	0.5		0.35	0.55	mA
			Full range			0.7			0.55			0.6	

† Full range is 0°C to 70°C.
‡ All typical values are at $T_A = 25$°C.

electrical characteristics at specified free-air temperature, V_{CC+} = 5 V, V_{CC-} = 0, V_O = 1.4 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013C			LT1013AC			LT1013DC			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		90	450		60	250		250	950	μV
			Full range			570			350			1200	
I_{IO}	Input offset current		25°C		0.3	2		0.2	1.3		0.3	2	nA
			Full range			6			3.5			6	
I_{IB}	Input bias current		25°C		−18	−50		−15	−35		−18	−50	nA
			Full range			−90			−55			−90	
V_{ICR}	Common-mode input voltage range		25°C	0 to 3.5	−0.3 to 3.8		0 to 3.5	−0.3 to 3.8		0 to 3.5	−0.3 to 3.8		V
			Full range	0 to 3			0 to 3			0 to 3			
V_{OM}	Maximum peak output voltage swing	Output low, No load	25°C		15	25		15	25		15	25	mV
		Output low, R_L = 600 Ω to GND	25°C		5	10		5	10		5	10	
			Full range			13			13			13	
		Output low, I_{sink} = 1 mA	25°C		220	350		220	350		220	350	
		Output high, No load	25°C	4	4.4		4	4.4		4	4.4		V
		Output high, R_L = 600 Ω to GND	25°C	3.4	4		3.4	4		3.4	4		
			Full range	3.2			3.3			3.2			
A_{VD}	Large-signal differential voltage amplification	V_O = 5 mV to 4 V, R_L = 500 Ω	25°C		1			1			1		V/μV
I_{CC}	Supply current per amplifier		25°C		0.32	0.5		0.31	0.45		0.32	0.5	mA
			Full range			0.55			0.5			0.55	

† Full range is 0°C to 70°C.
‡ All typical values are at T_A = 25°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, V_{IC} = 0, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		0.2	0.4		V/μs
V_n	Equivalent input noise voltage	f = 10 Hz		24		$nV/\sqrt{Hz}$
		f = 1 kHz		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.55		μV
I_n	Equivalent input noise current	f = 10 Hz		0.07		$pA/\sqrt{Hz}$

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V, $V_{IC} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013I			LT1013AI			LT1013DI			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$	25°C		60	300		40	150		200	800	μV
			Full range			550			300			1000	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage		Full range		0.4	2.5		0.3	2		0.7	5	μV/°C
	Long-term drift of input offset voltage		25°C		0.5			0.4			0.5		μV/mo
I_{IO}	Input offset current		25°C		0.2	1.5		0.15	0.8		0.2	1.5	nA
			Full range			2.8			1.5			2.8	
I_{IB}	Input bias current		25°C		−15	−30		−12	−20		−15	−30	nA
			Full range			−38			−25			−38	
V_{ICR}	Common-mode input voltage range		25°C	−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		V
			Full range	−15 to 13			−15 to 13			−15 to 13			
V_{OM}	Maximum peak output voltage swing	$R_L = 2\ k\Omega$	25°C	±12.5	±14		±13	±14		±12.5	±14		V
			Full range	±12			±12.5			±12			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V, $R_L = 600\ \Omega$	25°C	0.5	0.2		0.8	2.5		0.5	2		V/μV
		$V_O = \pm10$ V, $R_L = 2\ k\Omega$	25°C	1.2	7		1.5	8		1.2	7		
			Full range	0.7			1			0.7			
CMRR	Common-mode rejection ratio	$V_{IC} = -15$ V to 13.5 V	25°C	97	114		100	117		97	114		dB
		$V_{IC} = -14.9$ V to 13 V	Full range	94			97			94			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm} = \pm2$ V to ±18 V	25°C	100	117		103	120		100	117		dB
			Full range	97			101			97			
	Channel separation	$V_O = \pm10$ V, $R_L = 2\ k\Omega$	25°C	120	137		123	140		120	137		dB
r_{id}	Differential input resistance		25°C	70	300		100	400		70	300		MΩ
r_{ic}	Common-mode input resistance		25°C		4			5			4		GΩ
I_{CC}	Supply current per amplifier		25°C		0.35	0.55		0.35	0.5		0.35	0.55	mA
			Full range			0.7			0.55			0.6	

† Full range is −40°C to 105°C.
‡ All typical values are at $T_A = 25°C$.

electrical characteristics at specified free-air temperature, $V_{CC+} = 5$ V, $V_{CC-} = 0$, $V_O = 1.4$ V, $V_{IC} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013I			LT1013AI			LT1013DI			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$	25°C		90	450		60	250		250	950	μV
			Full range			570			350			1200	
I_{IO}	Input offset current		25°C		0.3	2		0.2	1.3		0.3	2	nA
			Full range			6			3.5			6	
I_{IB}	Input bias current		25°C		−18	−50		−15	−35		−18	−50	nA
			Full range			−90			−55			−90	
V_{ICR}	Common-mode input voltage range		25°C	0 to 3.5	−0.3 to 3.8		0 to 3.5	−0.3 to 3.8		0 to 3.5	−0.3 to 3.8		V
			Full range	0 to 3			0 to 3			0 to 3			
V_{OM}	Maximum peak output voltage swing	Output low, No load	25°C		15	25		15	25		15	25	mV
		Output low, $R_L = 600\ \Omega$ to GND	25°C		5	10		5	10		5	10	
			Full range			13			13			13	
		Output low, $I_{sink} = 1$ mA	25°C		220	350		220	350		220	350	
		Output high, No load	25°C	4	4.4		4	4.4		4	4.4		V
		Output high, $R_L = 600\ \Omega$ to GND	25°C	3.4	4		3.4	4		3.4	4		
			Full range	3.2			3.3			3.2			
A_{VD}	Large-signal differential voltage amplification	$V_O = 5$ mV to 4 V, $R_L = 500\ \Omega$	25°C		1			1			1		V/μV
I_{CC}	Supply current per amplifier		25°C		0.32	0.5		0.31	0.45		0.32	0.5	mA
			Full range			0.55			0.5			0.55	

† Full range is −40°C to 105°C.
‡ All typical values are at $T_A = 25$°C.

operating characteristics, $V_{CC\pm} = \pm15$ V, $V_{IC} = 0$, $T_A = 25$°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		0.2	0.4		V/μs
V_n	Equivalent input noise voltage	f = 10 Hz		24		$nV/\sqrt{Hz}$
		f = 1 kHz		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.55		μV
I_n	Equivalent input noise current	f = 10 Hz		0.07		$pA/\sqrt{Hz}$

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V, $V_{IC} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013M			LT1013AM			LT1013DM			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$	25°C		60	300		40	150		200	800	μV
			Full range			550			300			1000	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage		Full range		0.5	2.5*		0.4	2*		0.5	2.5*	μV/°C
	Long-term drift of input offset voltage		25°C		0.5			0.4			0.5		μV/mo
I_{IO}	Input offset current		25°C		0.2	1.5		0.15	0.8		0.2	1.5	nA
			Full range			5			2.5			5	
I_{IB}	Input bias current		25°C		−15	−30		−12	−20		−15	−30	nA
			Full range			−45			−30			−45	
V_{ICR}	Common-mode input voltage range		25°C	−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		V
			Full range	−14.9 to 13			−14.9 to 13			−14.9 to 13			
V_{OM}	Maximum peak output voltage swing	$R_L = 2\ k\Omega$	25°C	±12.5	±14		±13	±14		±12.5	±14		V
			Full range	±11.5			±12			±11.5			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V, $R_L = 600\ \Omega$	25°C	0.5	2		0.8	2.5		0.5	2		V/μV
		$V_O = +10$ V, $R_L = 2\ k\Omega$	25°C	1.2	7		1.5	8		1.2	7		
			Full range	0.25			0.5			0.25			
CMRR	Common-mode rejection ratio	$V_{IC} = -15$ V to 13.5 V	25°C	97	117		100	117		97	114		dB
		$V_{IC} = -14.9$ V to 13 V	Full range	94			97			94			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm} = \pm2$ V to ±18 V	25°C	100	117		103	120		100	117		dB
			Full range	97			100			97			
	Channel separation	$V_O = \pm10$ V, $R_L = 2\ k\Omega$	25°C	120	137		123	140		120	137		dB
r_{id}	Differential input resistance		25°C	70	300		100	400		70	300		MΩ
r_{ic}	Common-mode input resistance		25°C		4			5			4		GΩ
I_{CC}	Supply current per amplifier		25°C		0.35	0.55		0.35	0.5		0.35	0.55	mA
			Full range			0.7			0.6			0.7	

* On products compliant to MIL-PRF-38535, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.
‡ All typical values are at $T_A = 25$°C.

electrical characteristics at specified free-air temperature, V_{CC+} = 5 V, V_{CC-} = 0, V_O = 1.4 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013M			LT1013AM			LT1013DM			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		90	450		60	250		250	950	μV
			Full range		400	1500		250	900		800	2000	
		R_S = 50 Ω, V_{IC} = 0.1 V	125°C		200	750		120	450		560	1200	
I_{IO}	Input offset current		25°C		0.3	2		0.2	1.3		0.3	2	nA
			Full range			10			6			10	
I_{IB}	Input bias current		25°C		−18	−50		−15	−35		−18	−50	nA
			Full range			−120			−80			−120	
V_{ICR}	Common-mode input voltage range		25°C	0 to 3.5	−0.3 to 3.8		0 to 3.5	−0.3 to 3.8		0 to 3.5	−0.3 to 3.8		V
			Full range	0 to 3			0 to 3			0 to 3			
V_{OM}	Maximum peak output voltage swing	Output low, No load	25°C		15	25		15	25		15	25	mV
		Output low, R_L = 600 Ω to GND	25°C		5	10		5	10		5	10	
			Full range			18			15			18	
		Output low, I_{sink} = 1 mA	25°C		220	350		220	350		220	350	
		Output high, No load	25°C	4	4.4		4	4.4		4	4.4		V
		Output high, R_L = 600 Ω to GND	25°C	3.4	4		3.4	4		3.4	4		
			Full range	3.1			3.2			3.1			
A_{VD}	Large-signal differential voltage amplification	V_O = 5 mV to 4 V, R_L = 500 Ω	25°C		1			1			1		V/μV
I_{CC}	Supply current per amplifier		25°C		0.32	0.5		0.31	0.45		0.32	0.5	mA
			Full range			0.65			0.55			0.65	

† Full range is −55°C to 125°C.
‡ All typical values are at T_A = 25°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, V_{IC} = 0, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		0.2	0.4		V/μs
V_n	Equivalent input noise voltage	f = 10 Hz		24		nV/√Hz
		f = 1 kHz		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.55		μV
I_n	Equivalent input noise current	f = 10 Hz		0.07		pA/√Hz

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Supply voltage	1
		vs Temperature	2
ΔV_{IO}	Change in input offset voltage	vs Time	3
I_{IO}	Input offset current	vs Temperature	4
I_{IB}	Input bias current	vs Temperature	5
V_{IC}	Common-mode input voltage	vs Input bias current	6
A_{VD}	Differential voltage amplification	vs Load resistance	7, 8
		vs Frequency	9, 10
	Channel separation	vs Frequency	11
	Output saturation voltage	vs Temperature	12
CMRR	Common-mode rejection ratio	vs Frequency	13
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	14
I_{CC}	Supply current	vs Temperature	15
I_{OS}	Short-circuit output current	vs Time	16
V_n	Equivalent input noise voltage	vs Frequency	17
I_n	Equivalent input noise current	vs Frequency	17
$V_{N(PP)}$	Peak-to-peak input noise voltage	vs Time	18
	Pulse response	Small signal	19, 21
		Large signal	20, 22, 23
	Phase shift	vs Frequency	9

TYPICAL CHARACTERISTICS†

INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE

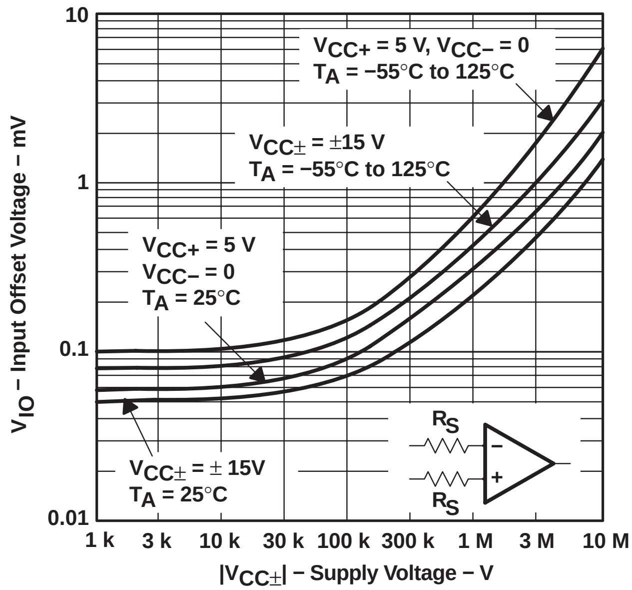


Figure 1

INPUT OFFSET VOLTAGE OF REPRESENTATIVE UNITS vs FREE-AIR TEMPERATURE

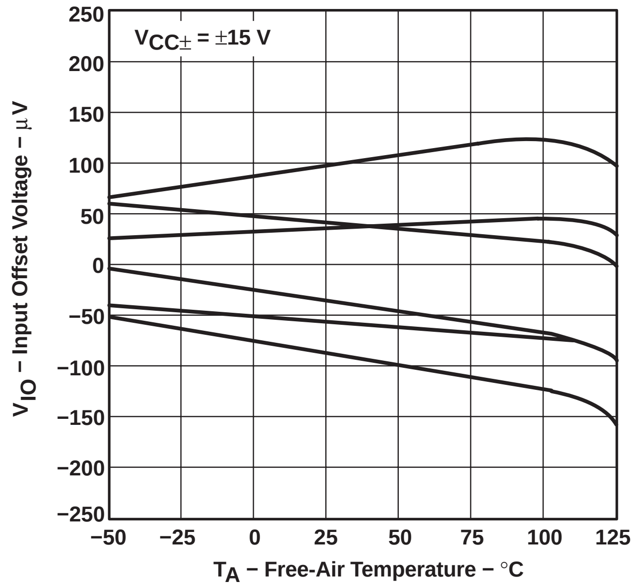


Figure 2

WARM-UP CHANGE IN INPUT OFFSET VOLTAGE vs TIME AFTER POWER-ON

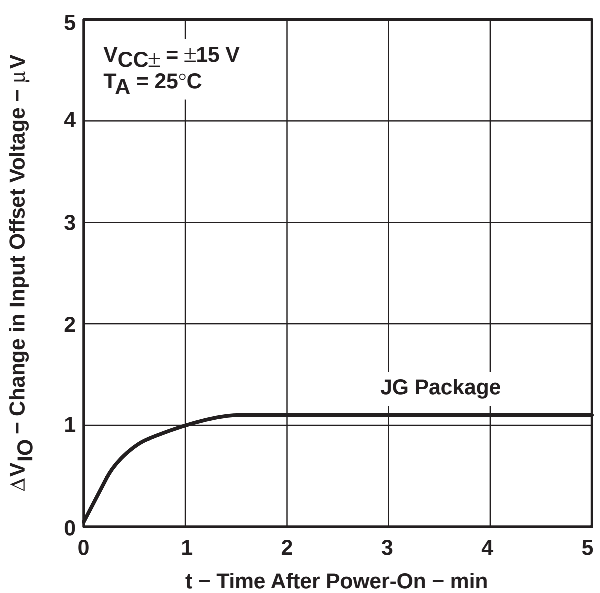


Figure 3

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

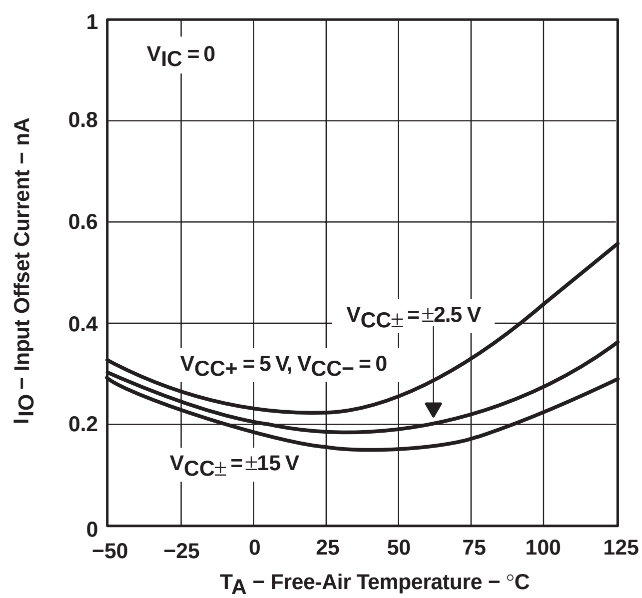


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

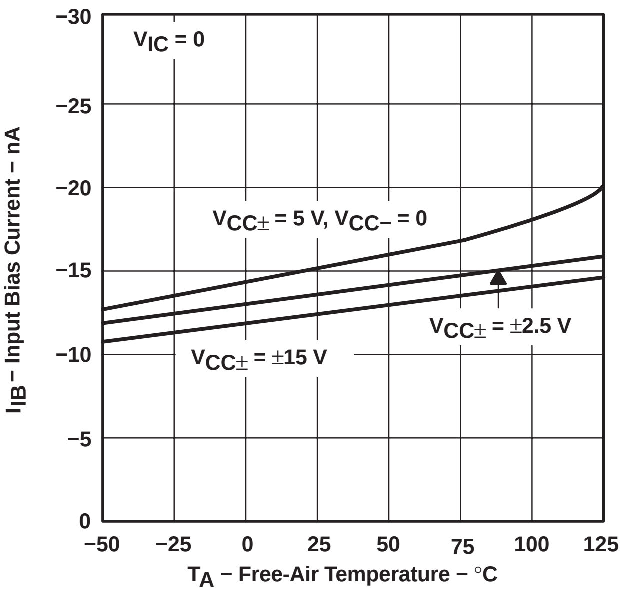


Figure 5

COMMON-MODE INPUT VOLTAGE
vs
INPUT BIAS CURRENT

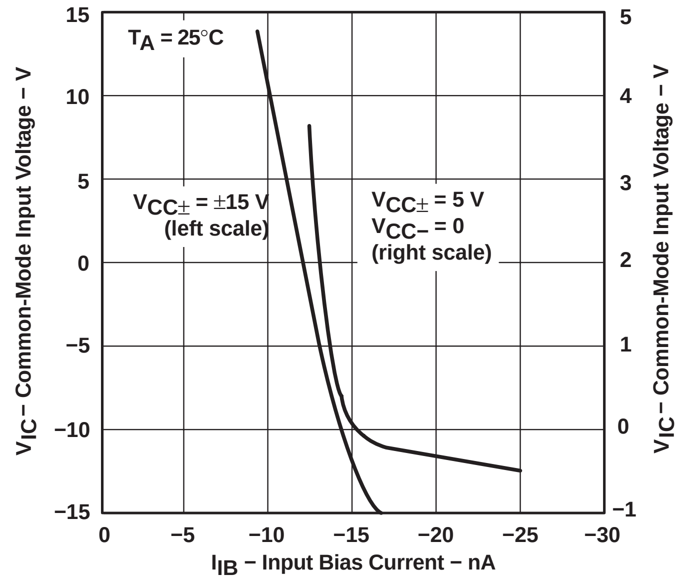


Figure 6

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

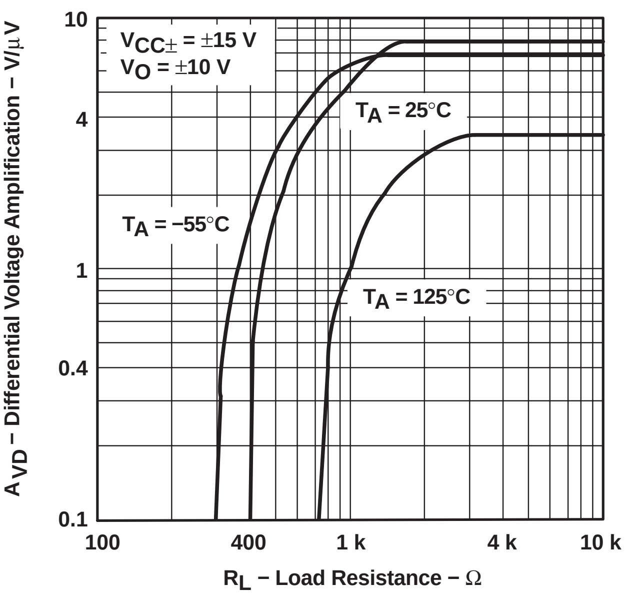


Figure 7

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

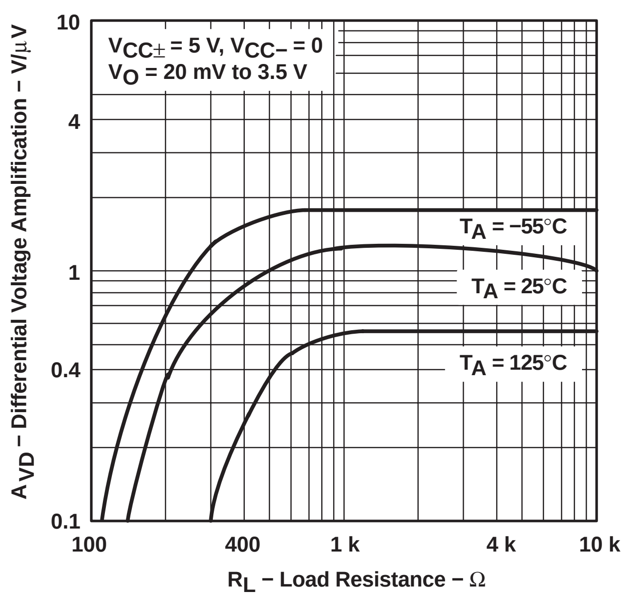


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

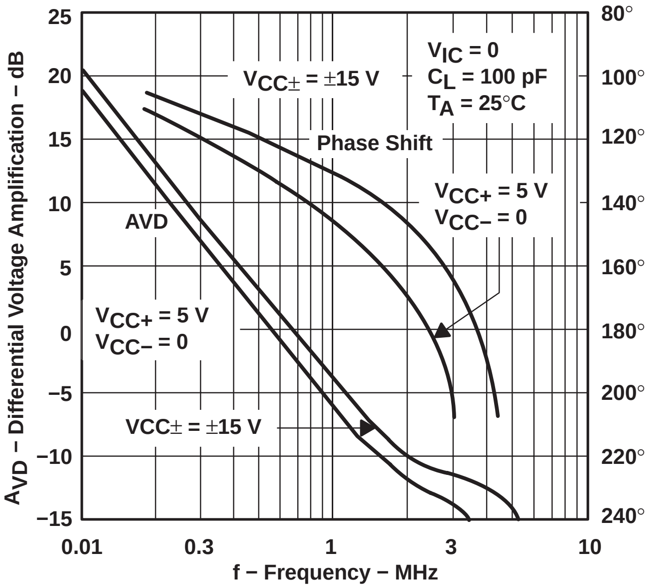


Figure 9

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

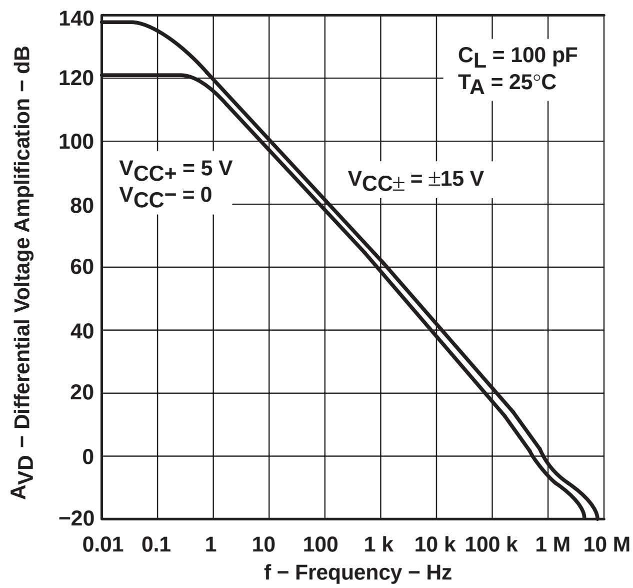


Figure 10

CHANNEL SEPARATION vs FREQUENCY

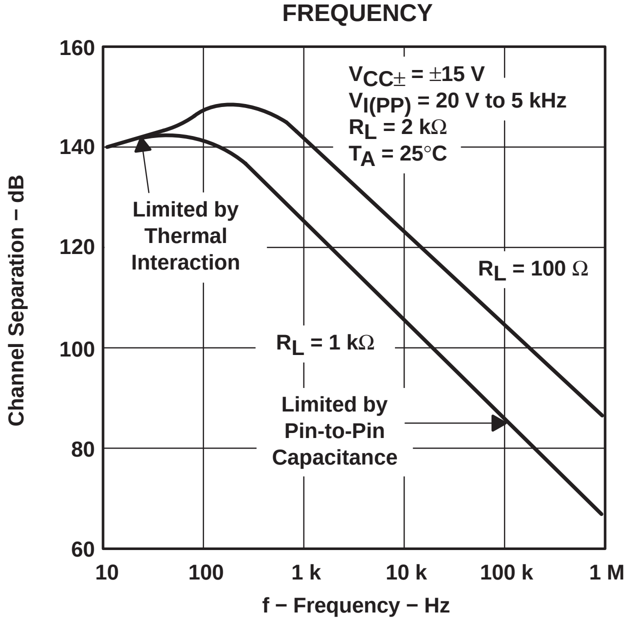


Figure 11

OUTPUT SATURATION VOLTAGE vs FREE-AIR TEMPERATURE

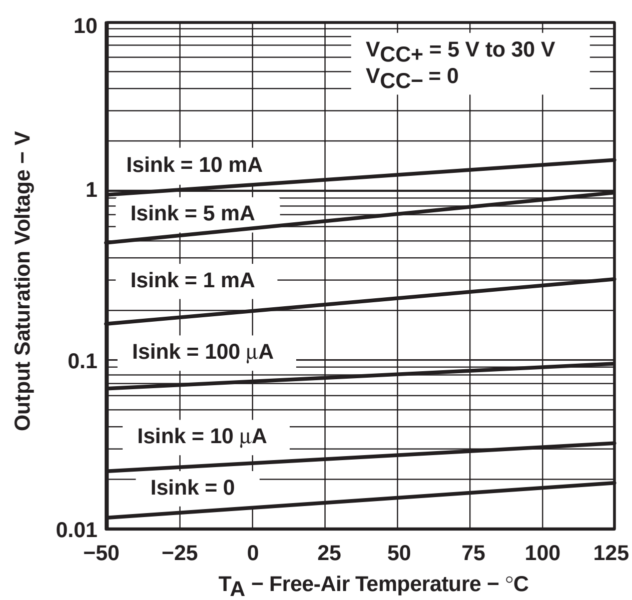


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

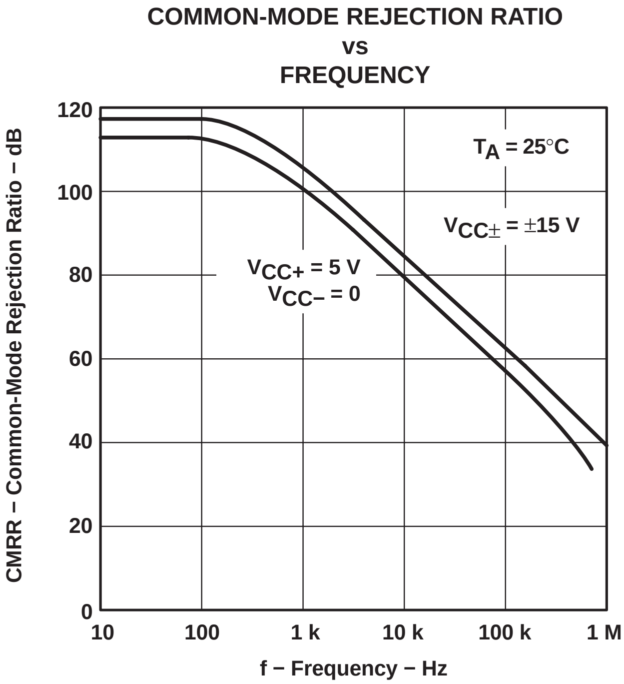


Figure 13

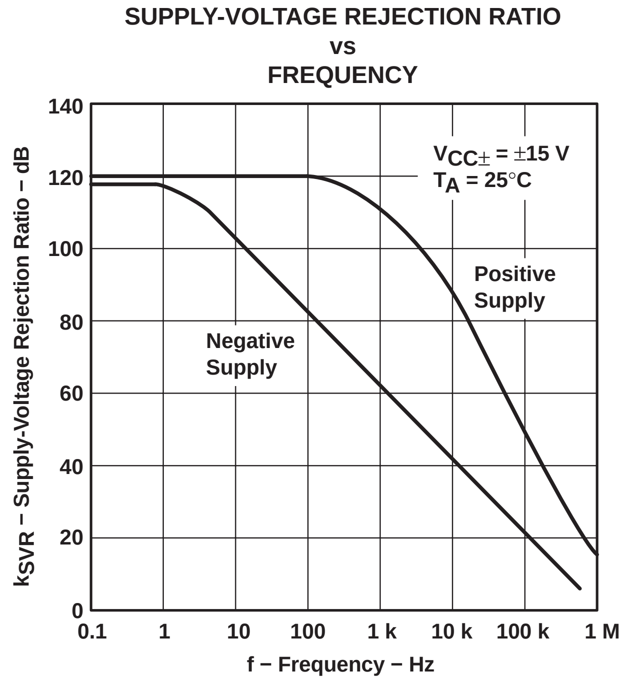


Figure 14

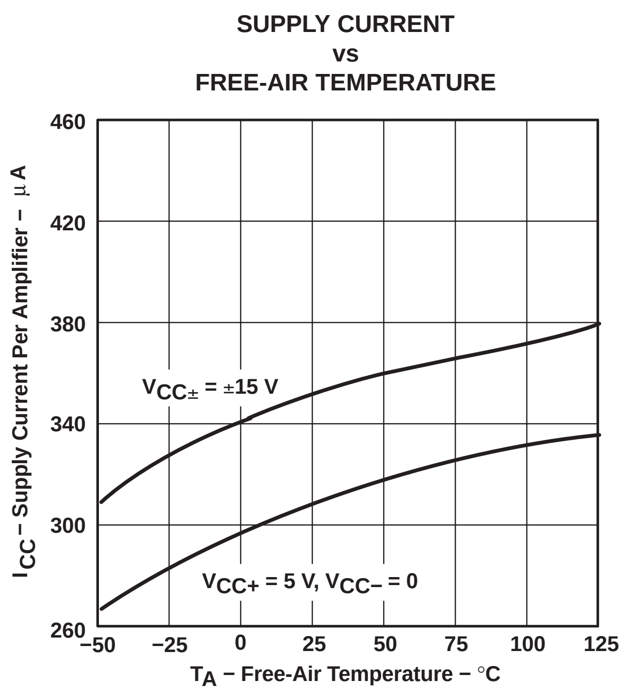


Figure 15

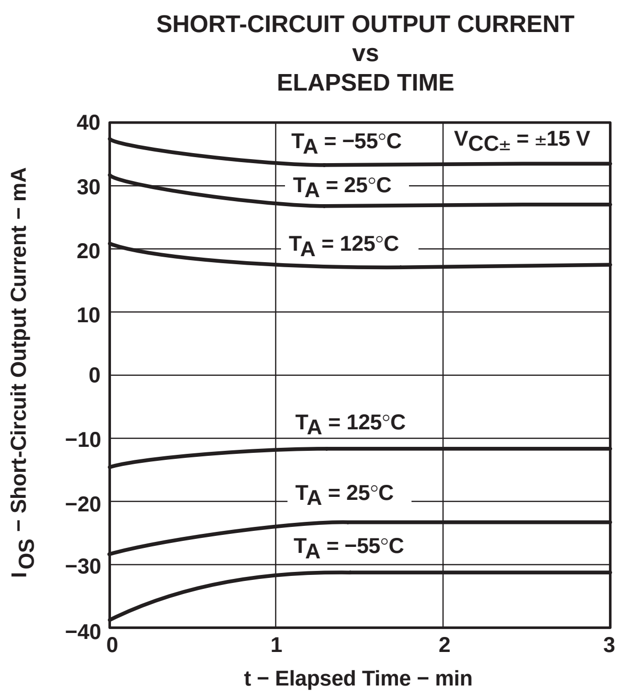


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE AND EQUIVALENT INPUT NOISE CURRENT vs FREQUENCY

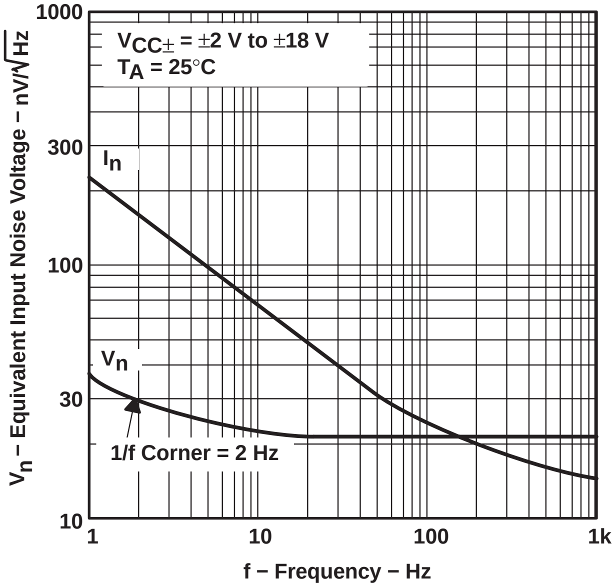


Figure 17

PEAK-TO-PEAK INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

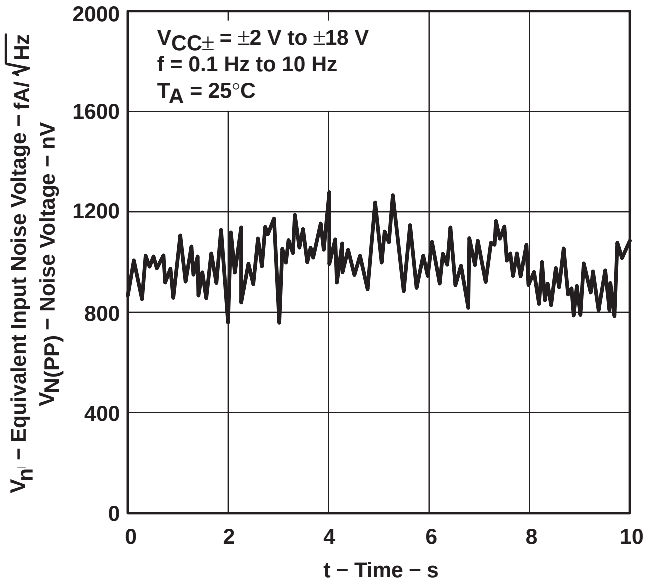


Figure 18

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

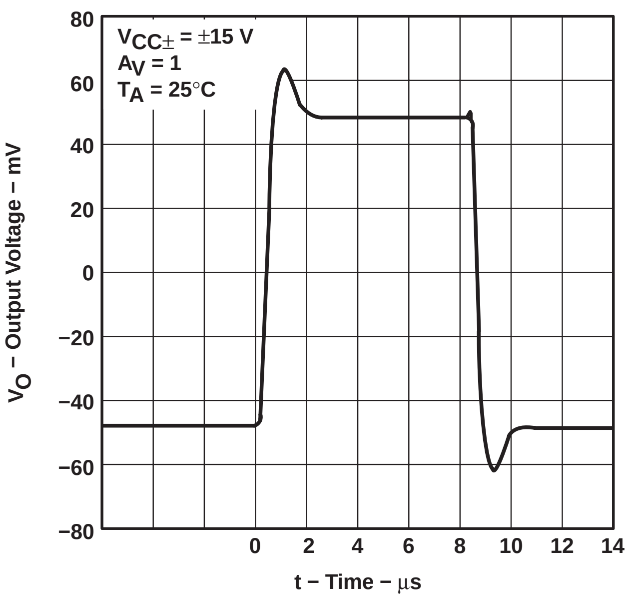


Figure 19

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

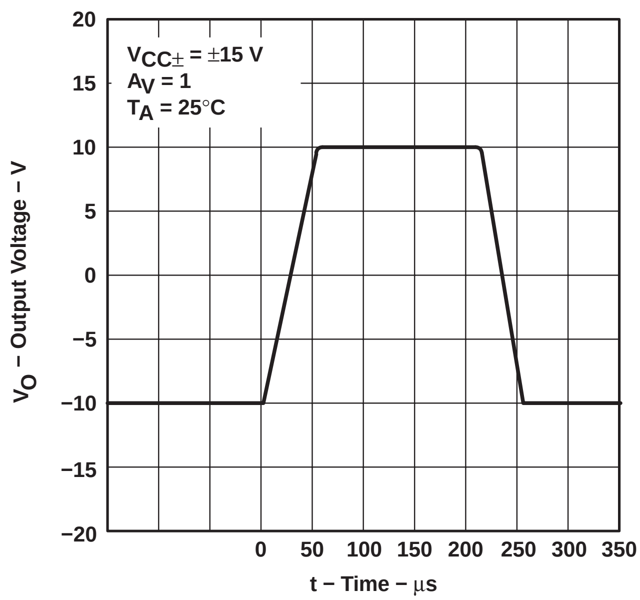


Figure 20

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

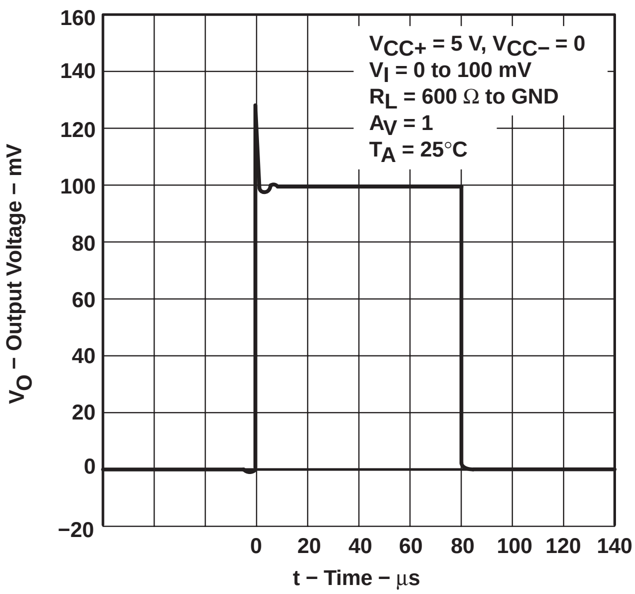


Figure 21

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

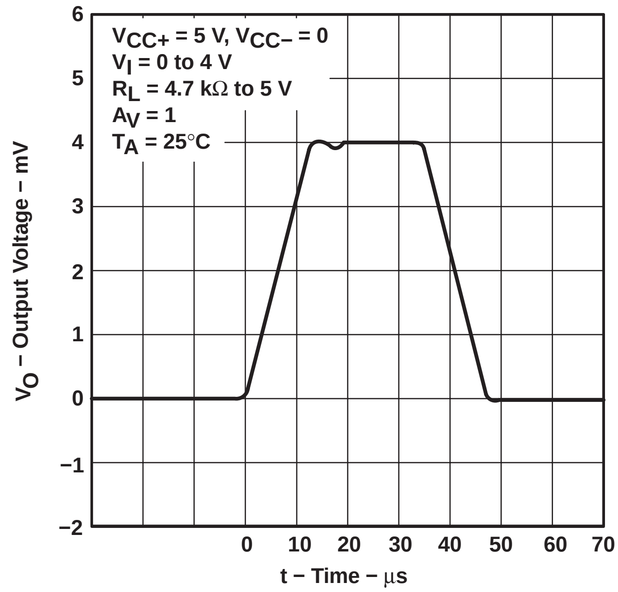


Figure 22

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

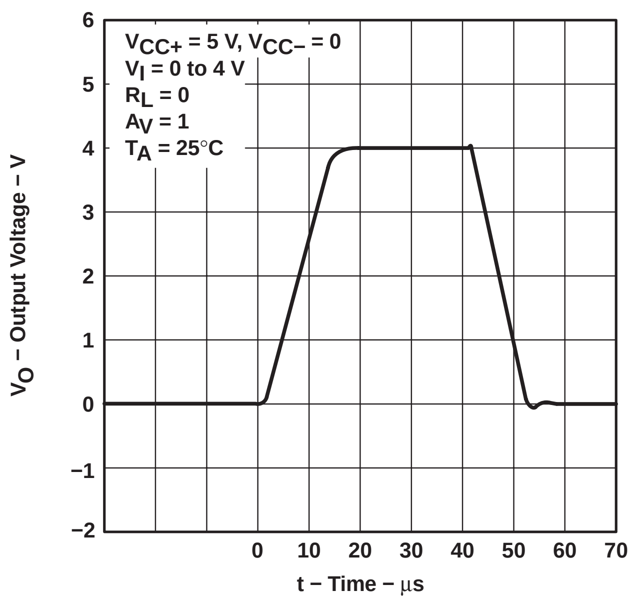


Figure 23

APPLICATION INFORMATION

single-supply operation

The LT1013 is fully specified for single-supply operation (V_{CC-} = 0). The common-mode input voltage range includes ground, and the output swings to within a few millivolts of ground.

Furthermore, the LT1013 has specific circuitry that addresses the difficulties of single-supply operation, both at the input and at the output. At the input, the driving signal can fall below 0 V, either inadvertently or on a transient basis. If the input is more than a few hundred millivolts below ground, the LT1013 is designed to deal with the following two problems that can occur:

1. On many other operational amplifiers, when the input is more than a diode drop below ground, unlimited current flows from the substrate (V_{CC-} terminal) to the input, which can destroy the unit. On the LT1013, the 400-Ω resistors in series with the input [see *schematic (each amplifier)*] protect the device, even when the input is 5 V below ground.
2. When the input is more than 400 mV below ground (at T_A = 25°C), the input stage of similar operational amplifiers saturates, and phase reversal occurs at the output. This can cause lockup in servo systems. Because of unique phase-reversal protection circuitry (Q21, Q22, Q27, and Q28), the LT1013 outputs do not reverse, even when the inputs are at −1.5 V (see Figure 24).

This phase-reversal protection circuitry does not function when the other operational amplifier on the LT1013 is driven hard into negative saturation at the output. Phase-reversal protection does not work on amplifier 1 when amplifier 2 output is in negative saturation nor on amplifier 2 when amplifier 1 output is in negative saturation.

At the output, other single-supply designs either cannot swing to within 600 mV of ground or cannot sink more than a few microamperes while swinging to ground. The all-npn output stage of the LT1013 maintains its low output resistance and high-gain characteristics until the output is saturated. In dual-supply operations, the output stage is free of crossover distortion.

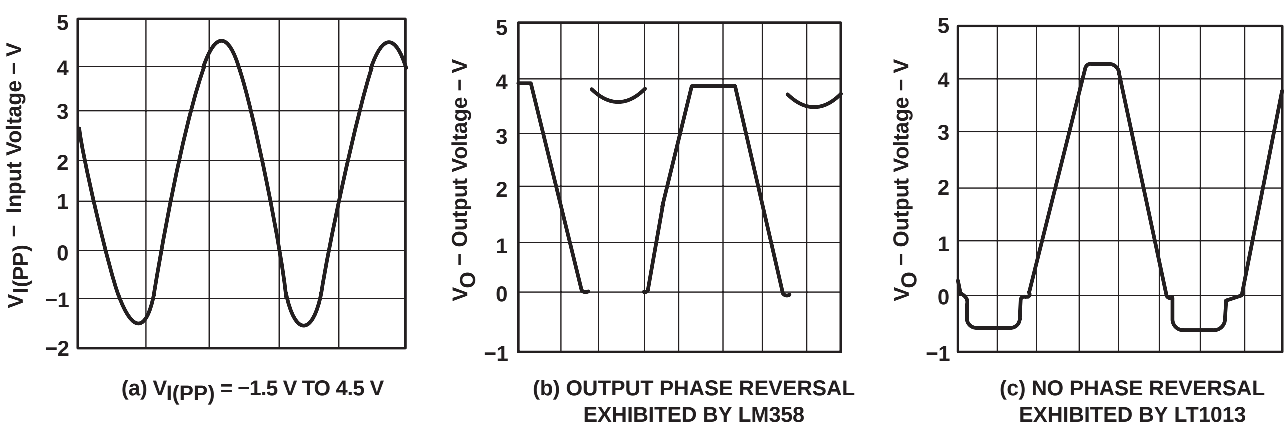


Figure 24. Voltage-Follower Response With Input Exceeding the Negative Common-Mode Input Voltage Range

APPLICATION INFORMATION

comparator applications

The single-supply operation of the LT1013 is well suited for use as a precision comparator with TTL-compatible output. In systems using both operational amplifiers and comparators, the LT1013 can perform multiple duties (see Figures 25 and 26).

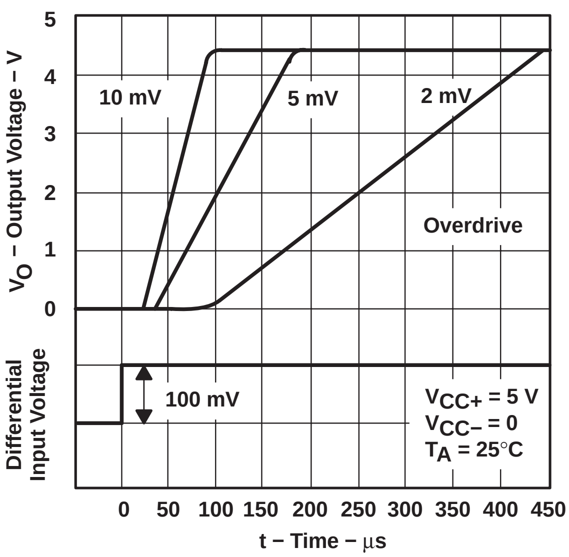


Figure 25. Low-to-High-Level Output Response for Various Input Overdrives

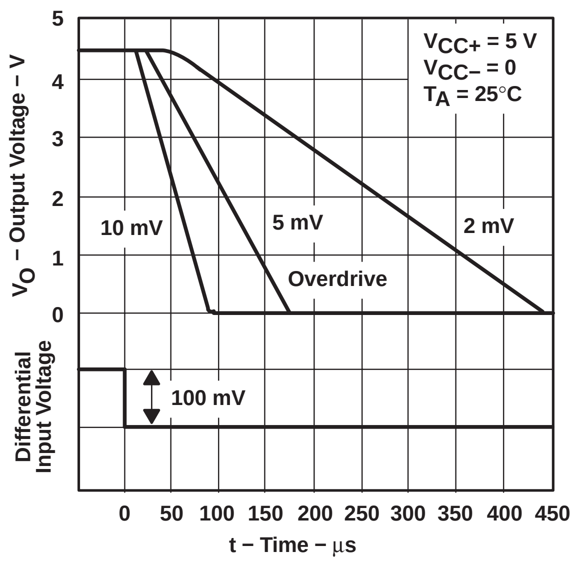


Figure 26. High-to-Low-Level Output Response for Various Input Overdrives

low-supply operation

The minimum supply voltage for proper operation of the LT1013 is 3.4 V (three NiCad batteries). Typical supply current at this voltage is 290 µA; therefore, power dissipation is only 1 mW per amplifier.

offset voltage and noise testing

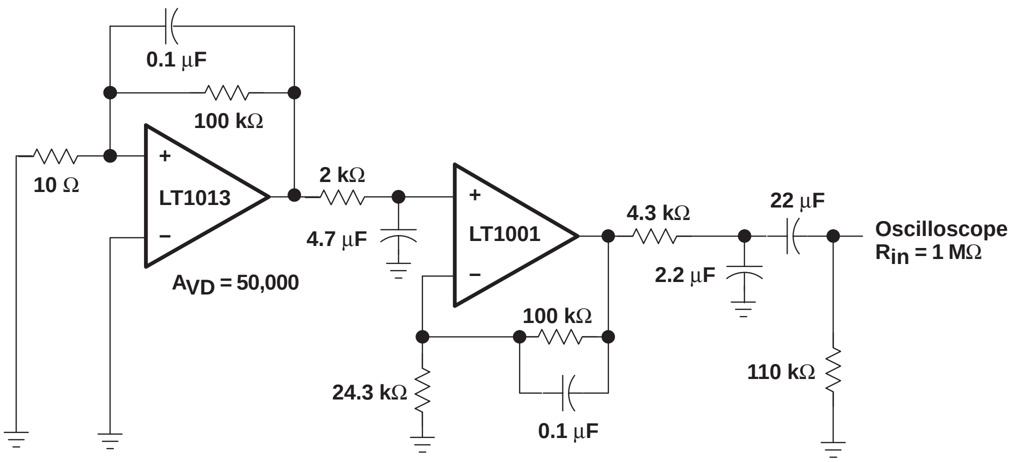
The test circuit for measuring input offset voltage and its temperature coefficient is shown in Figure 30. This circuit, with supply voltages increased to ±20 V, also is used as the burn-in configuration.

The peak-to-peak equivalent input noise voltage of the LT1013 is measured using the test circuit shown in Figure 27. The frequency response of the noise tester indicates that the 0.1-Hz corner is defined by only one zero. The test time to measure 0.1-Hz to 10-Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contribution from the frequency band below 0.1 Hz.

An input noise voltage test is recommended when measuring the noise of a large number of units. A 10-Hz input noise voltage measurement correlates well with a 0.1-Hz peak-to-peak noise reading because both results are determined by the white noise and the location of the 1/f corner frequency.

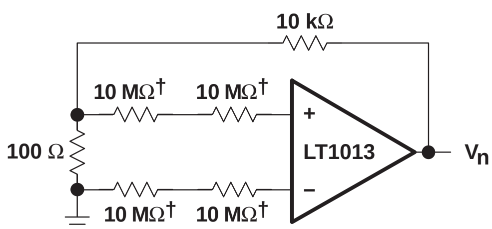
Current noise is measured by the circuit and formula shown in Figure 28. The noise of the source resistors is subtracted.

APPLICATION INFORMATION



NOTE A: All capacitor values are for nonpolarized capacitors only.

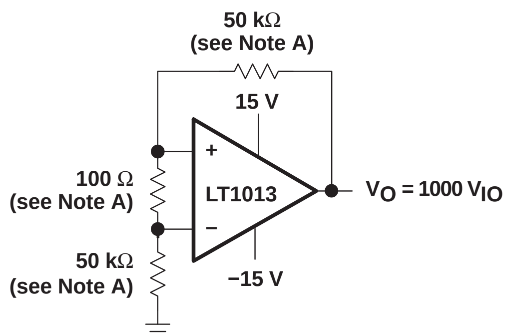
Figure 27. 0.1-Hz to 10-Hz Peak-to-Peak Noise Test Circuit



$$I_n = \frac{\left[V_{no}{}^2 - (820\ \text{nV})^2\right]^{1/2}}{40\ \text{M}\Omega \times 100}$$

† Metal-film resistor

Figure 28. Noise-Current Test Circuit and Formula

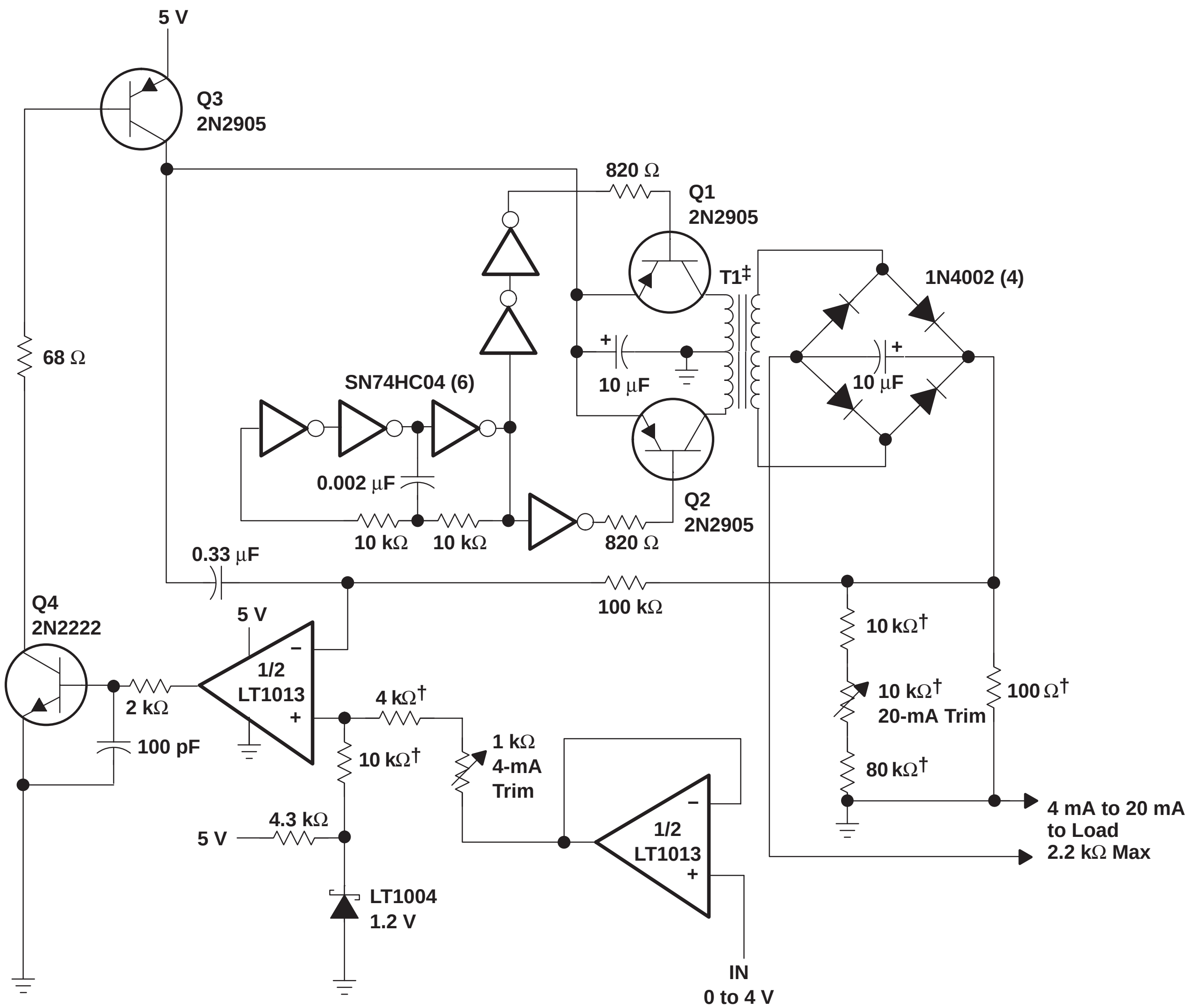


NOTE A: Resistors must have low thermoelectric potential.

Figure 29. Test Circuit for V_{IO} and $\alpha_{V_{IO}}$

APPLICATION INFORMATION

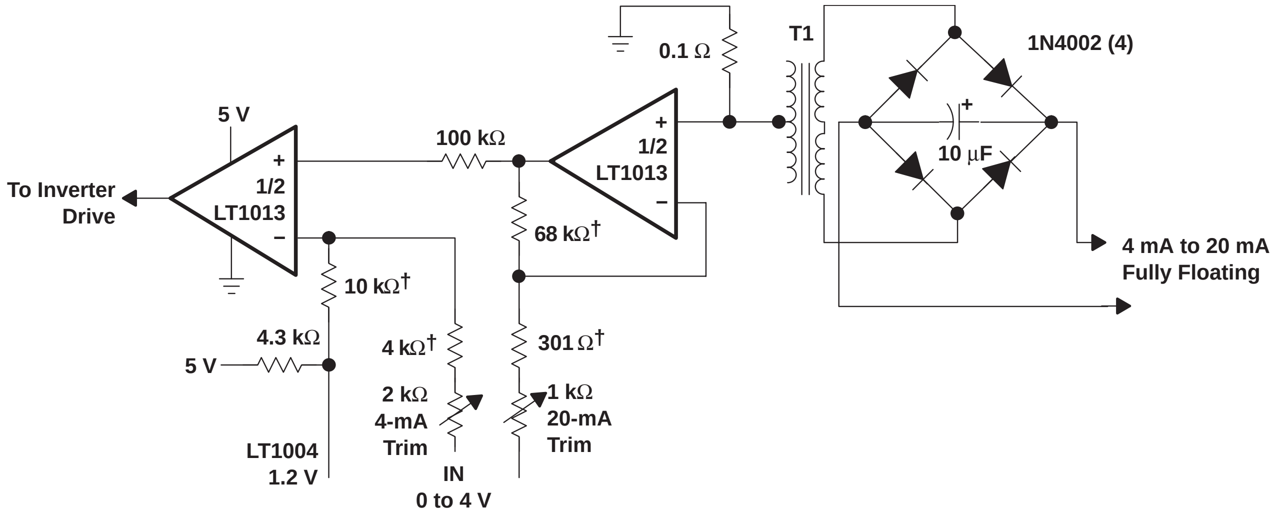
typical applications



† 1% film resistor. Match 10-kΩ resistors to within 0.05%.
‡ T1 = PICO-31080

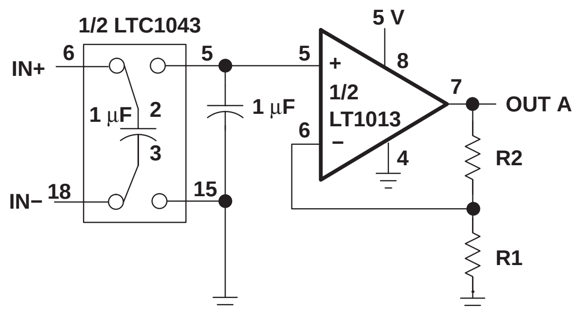
Figure 30. 5-V 4-mA to 20-mA Current-Loop Transmitter With 12-Bit Accuracy

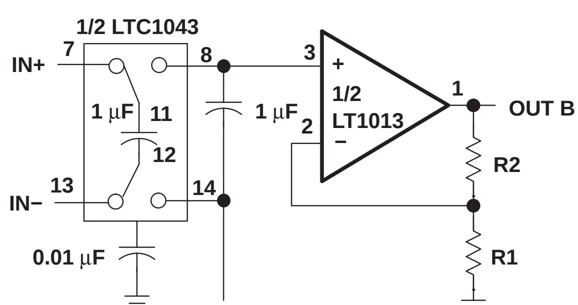
APPLICATION INFORMATION



† 1% film resistor

Figure 31. Fully Floating Modification to 4-mA to 20-mA Current-Loop Transmitter With 8-Bit Accuracy

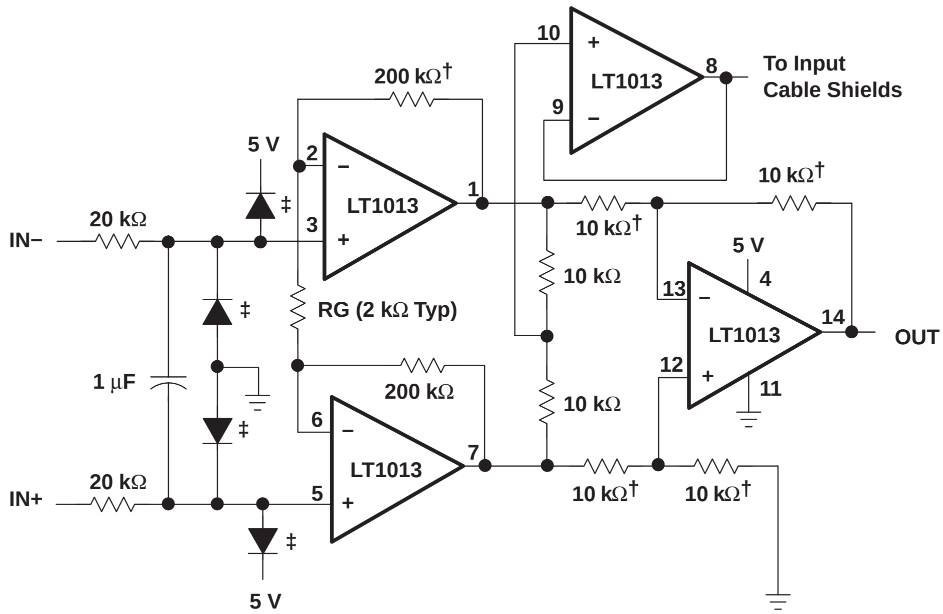




NOTE A: V_{IO} = 150 µV, A_{VD} = (R1/R2) + 1, CMRR = 120 dB, V_{ICR} = 0 to 5 V

Figure 32. 5-V Single-Supply Dual Instrumentation Amplifier

APPLICATION INFORMATION



† 1% film resistor. Match 10-kΩ resistors to within 0.05%.
‡ For high source impedances, use 2N2222 diodes.
NOTE A: A_{VD} = (400,000/RG) + 1

Figure 33. 5-V Precision Instrumentation Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-88760012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-88760012A LT1013AMFKB	Samples
5962-8876001PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8876001PA LT1013AM	Samples
5962-88760022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-88760022A LT1013MFKB	Samples
5962-8876002PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8876002PA LT1013M	Samples
LT1013AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-88760012A LT1013AMFKB	Samples
LT1013AMJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	LT1013AMJG	Samples
LT1013AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8876001PA LT1013AM	Samples
LT1013AMP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-55 to 125		
LT1013CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013C	Samples
LT1013CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013C	Samples
LT1013CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013C	Samples
LT1013CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013C	Samples
LT1013CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013C	Samples
LT1013CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LT1013CP	Samples
LT1013CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LT1013CP	Samples
LT1013DD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013D	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LT1013DDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013D	Samples
LT1013DDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013D	Samples
LT1013DDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013D	Samples
LT1013DDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013D	Samples
LT1013DID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1013DI	Samples
LT1013DIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1013DI	Samples
LT1013DIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1013DI	Samples
LT1013DIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1013DI	Samples
LT1013DIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1013DI	Samples
LT1013DIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1013DI	Samples
LT1013DIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	LT1013DIP	Samples
LT1013DIPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	LT1013DIP	Samples
LT1013DMD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	1013DM	Samples
LT1013DMDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	1013DM	Samples
LT1013DP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LT1013DP	Samples
LT1013DPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LT1013DP	Samples
LT1013IP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
LT1013MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-88760022A LT1013MFKB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LT1013MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	LT1013MJG	Samples
LT1013MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8876002PA LT1013M	Samples
LT1013MP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-55 to 125		
LT1013Y	OBSOLETE	DIESALE	Y	0		TBD	Call TI	Call TI			

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LT1013, LT1013M :

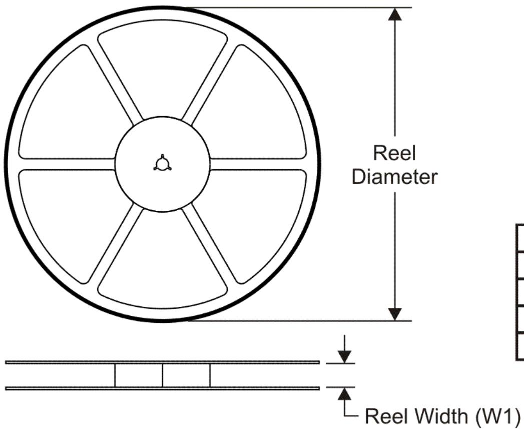
- Catalog: LT1013
- Military: LT1013M

NOTE: Qualified Version Definitions:

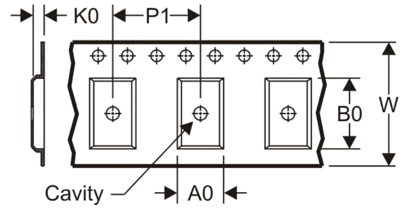
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

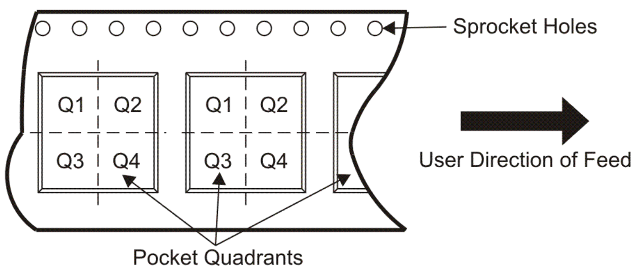


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

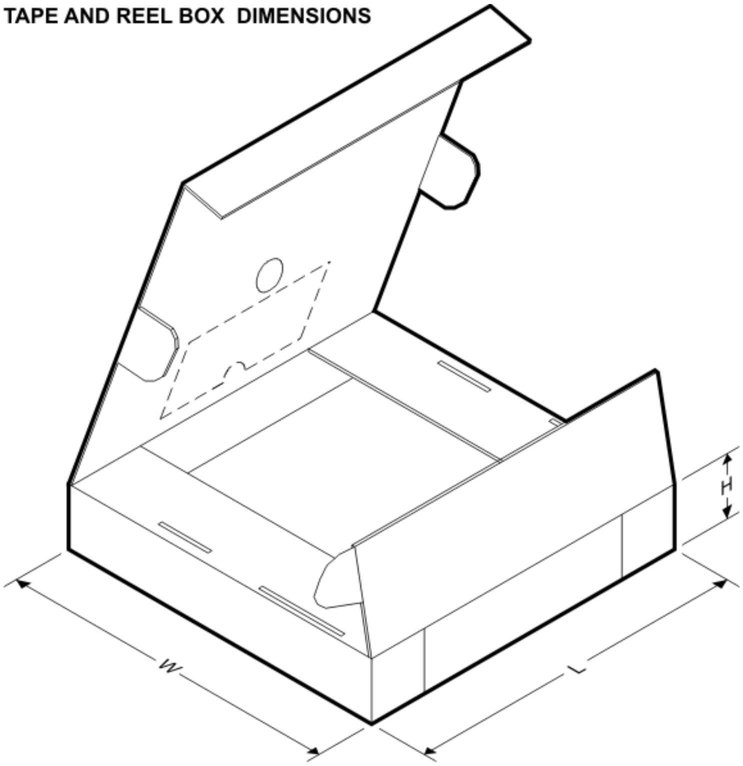
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LT1013CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1013DDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1013DIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

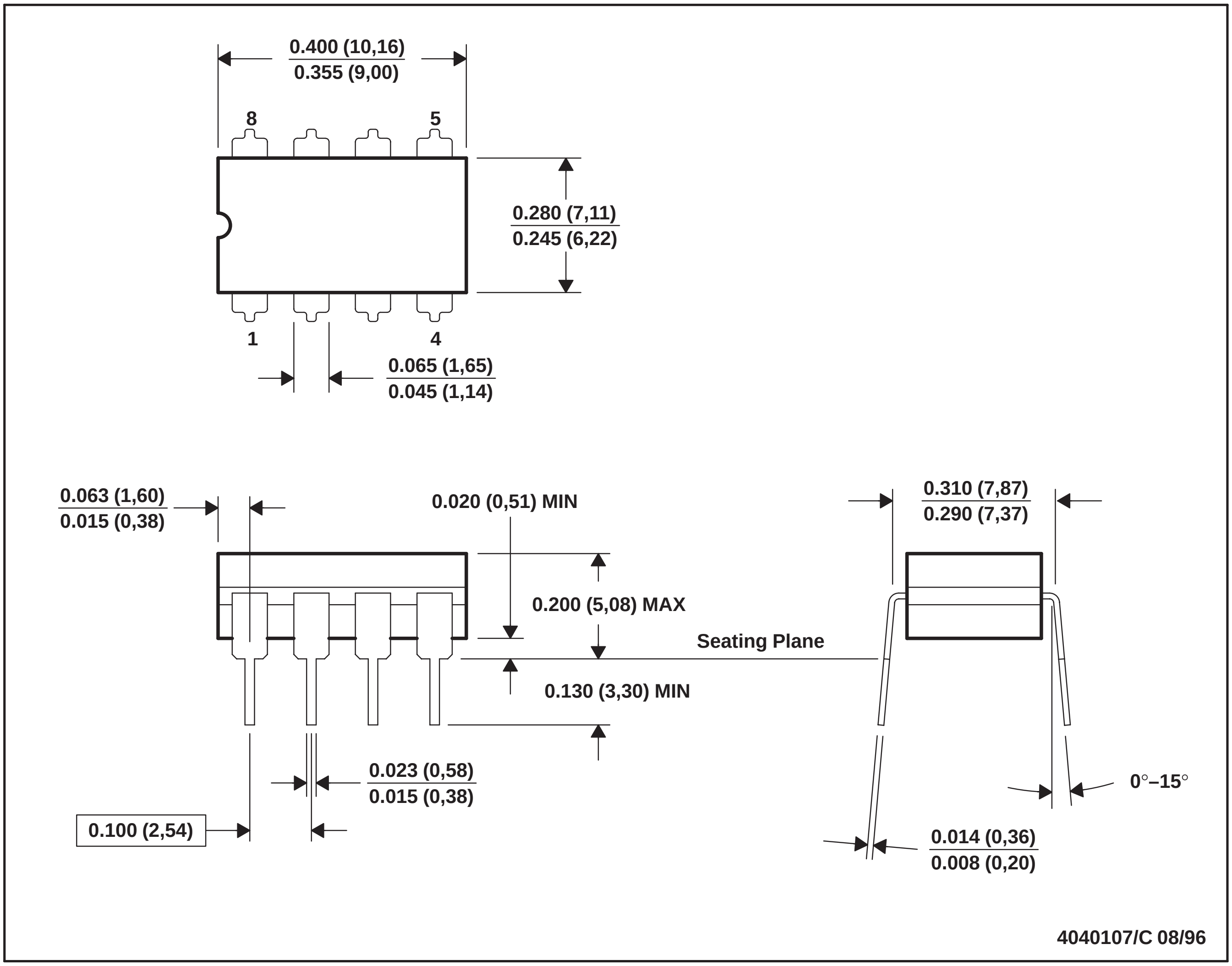
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LT1013CDR	SOIC	D	8	2500	340.5	338.1	20.6
LT1013DDR	SOIC	D	8	2500	340.5	338.1	20.6
LT1013DIDR	SOIC	D	8	2500	340.5	338.1	20.6

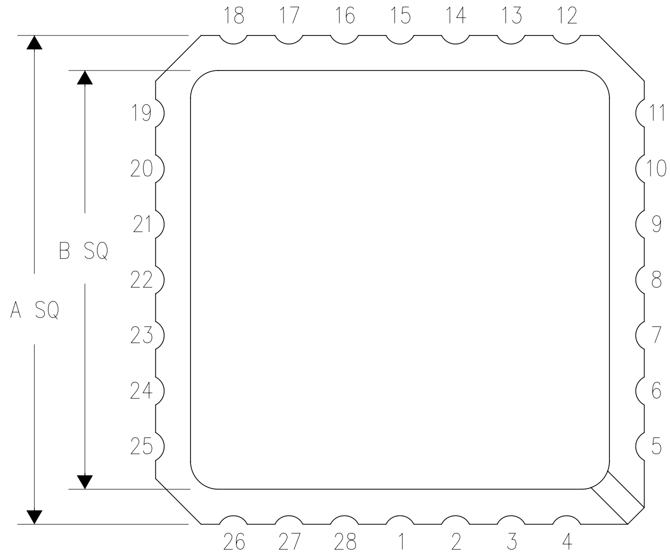
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



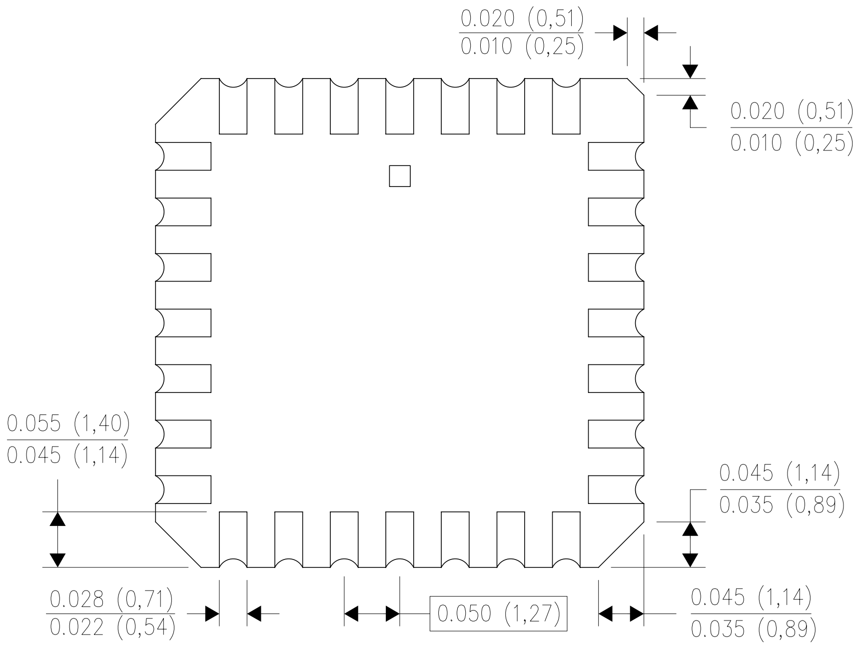
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP1-T8

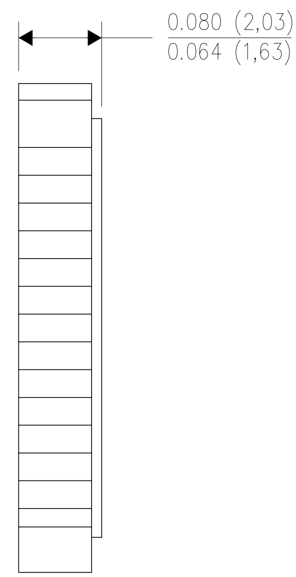
FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

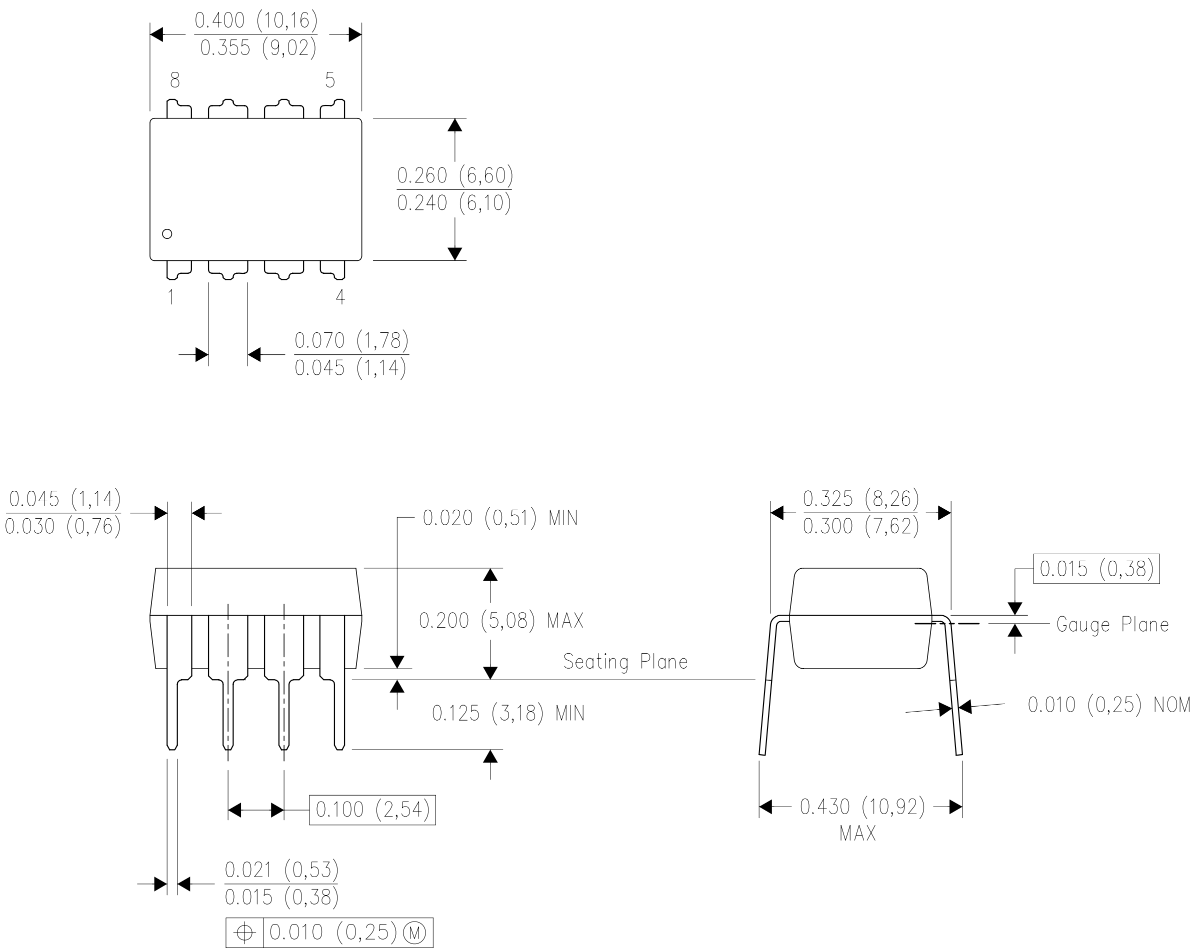




4040140/D 01/11

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS-004

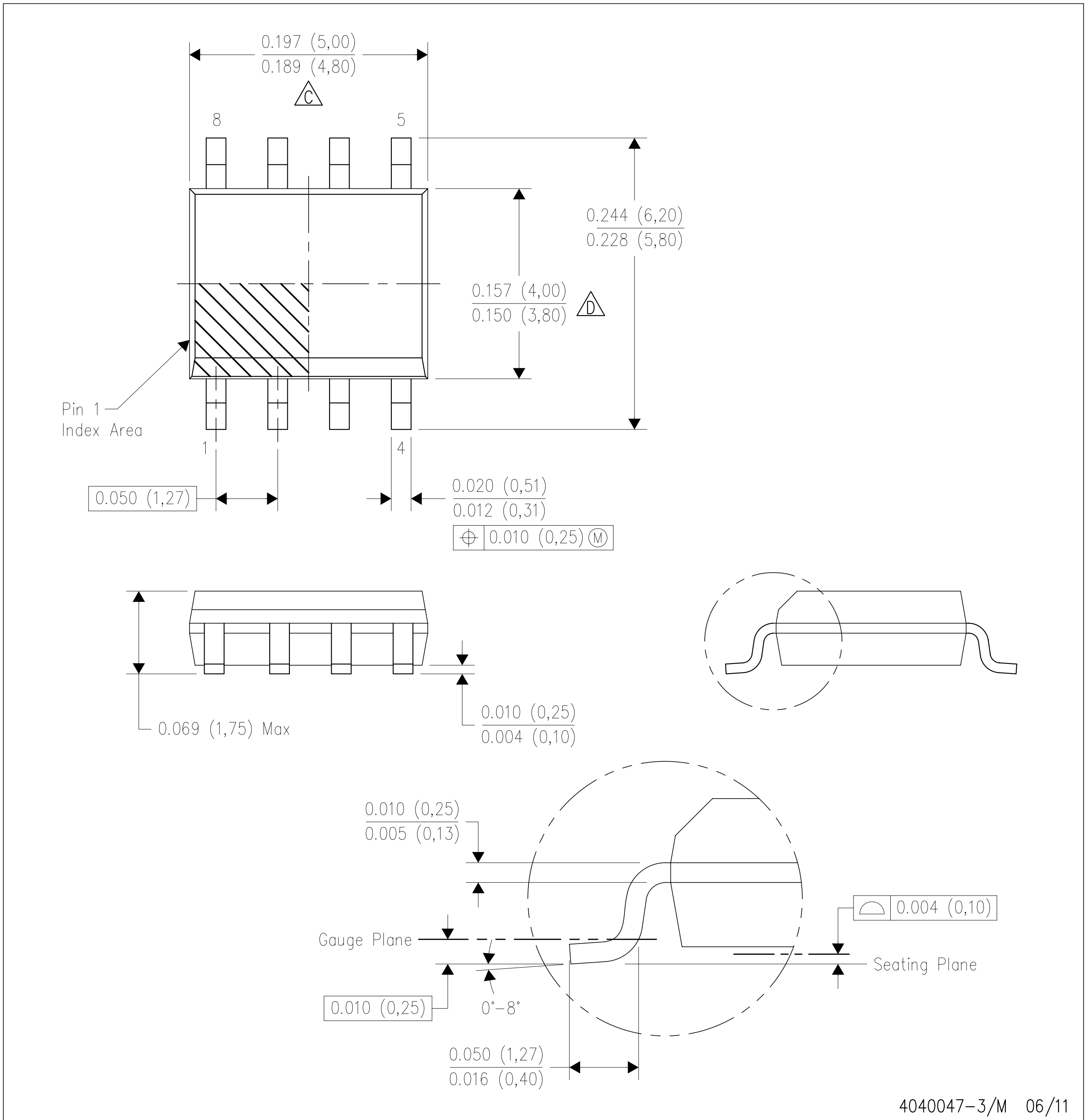
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

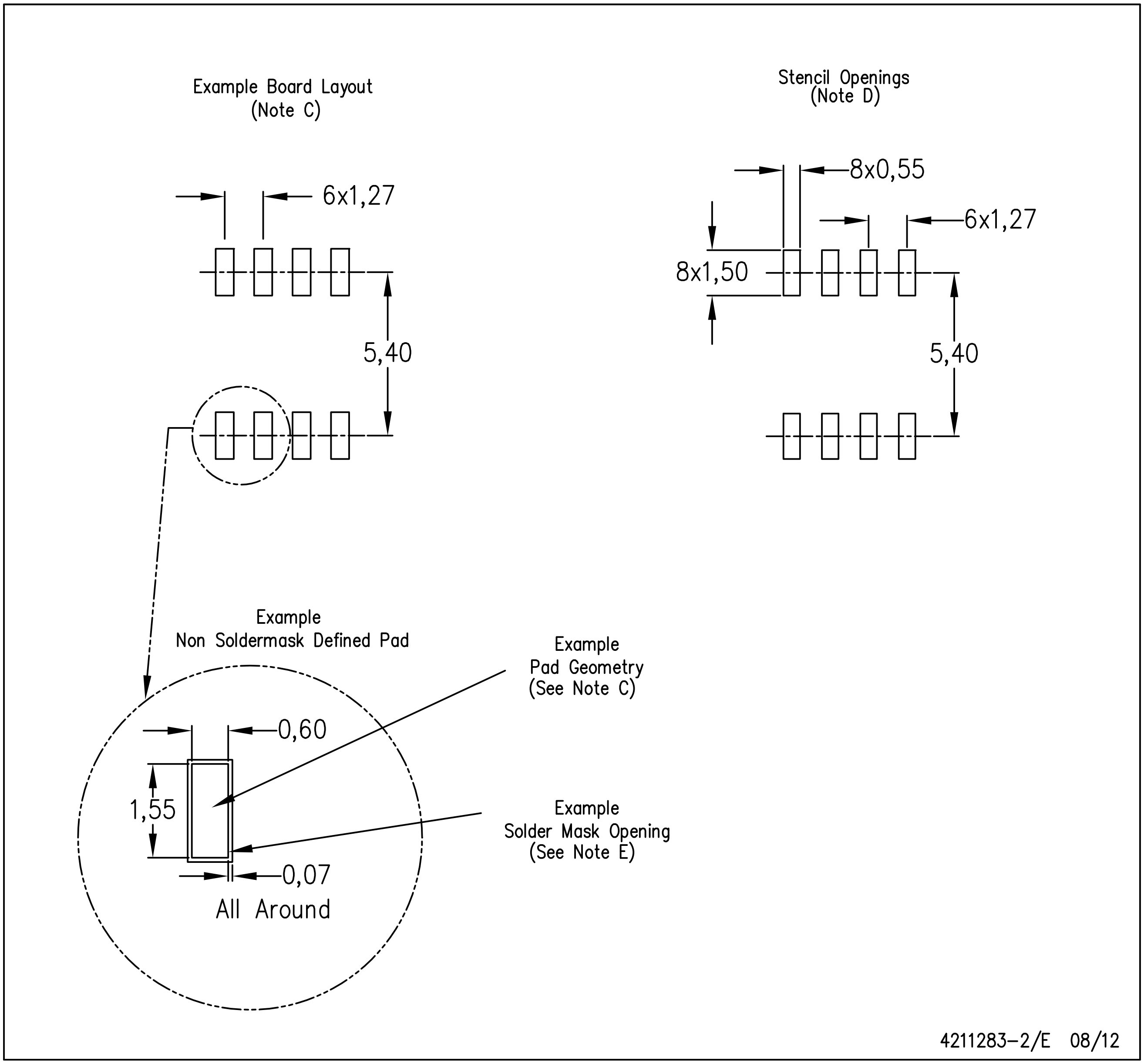
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.