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SN54LVCH244A, SN74LVCH244A
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS
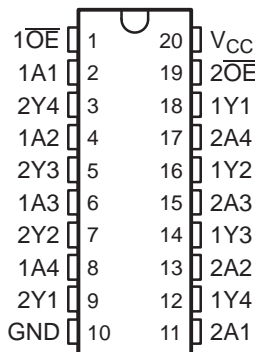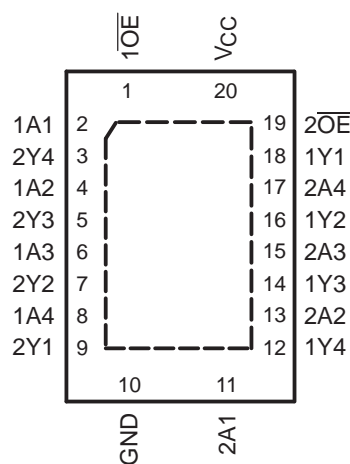SCES009O − JULY 1995 − REVISED FEBRUARY 2007

FEATURES

- **Operate From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 5.9 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**

- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
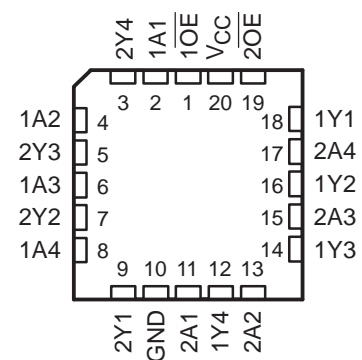 - **1000-V Charged-Device Model (C101)**

SN54LVCH244A . . . J OR W PACKAGE
SN74LVCH244A . . . DB, DBQ, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	20	V_{CC}
1A1	2	19	2$\overline{OE}$
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4
GND	10	11	2A1

SN74LVCH244A . . . RGY PACKAGE
(TOP VIEW)

Top: 1$\overline{OE}$ (1), V_{CC} (20)

1A1	2	19	2$\overline{OE}$
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4

Bottom: GND (10), 2A1 (11)

SN54LVCH244A . . . FK PACKAGE
(TOP VIEW)

Top pins: 2Y4 (3), 1A1 (2), 1$\overline{OE}$ (1), V_{CC} (20), 2$\overline{OE}$ (19)

1A2	4	18	1Y1
2Y3	5	17	2A4
1A3	6	16	1Y2
2Y2	7	15	2A3
1A4	8	14	1Y3

Bottom pins: 2Y1 (9), GND (10), 2A1 (11), 1Y4 (12), 2A2 (13)

DESCRIPTION/ORDERING INFORMATION

The SN54LVCH244A octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVCH244A octal buffer/line driver is designed for 1.65-V to 3.6-V V_{CC} operation.

These devices are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, these devices pass data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN54LVCH244A, SN74LVCH244A
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVCH244ARGYR	LCH244A
	SOIC – DW	Tube of 25	SN74LVCH244ADW	LVCH244A
		Reel of 2000	SN74LVCH244ADWR	
	SOP – NS	Reel of 2000	SN74LVCH244ANSR	LVCH244A
	SSOP – DB	Reel of 2000	SN74LVCH244ADBR	LCH244A
	SSOP (QSOP) – DBQ	Reel of 2500	SN74LVCH244ADBQR	LVCH244A
	TSSOP – PW	Tube of 70	SN74LVCH244APW	LCH244A
		Reel of 2000	SN74LVCH244APWR	
		Reel of 250	SN74LVCH244APWT	
	TVSOP – DGV	Reel of 2000	SN74LVCH244ADGVR	LCH244A
−55°C to 125°C	CDIP – J	Tube of 20	SNJ54LVCH244AJ	SNJ54LVCH244AJ
	CFP – W	Tube of 85	SNJ54LVCH244AW	SNJ54LVCH244AW
	LCCC – FK	Tube of 55	SNJ54LVCH244AFK	SNJ54LVCH244AFK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(EACH BUFFER)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)

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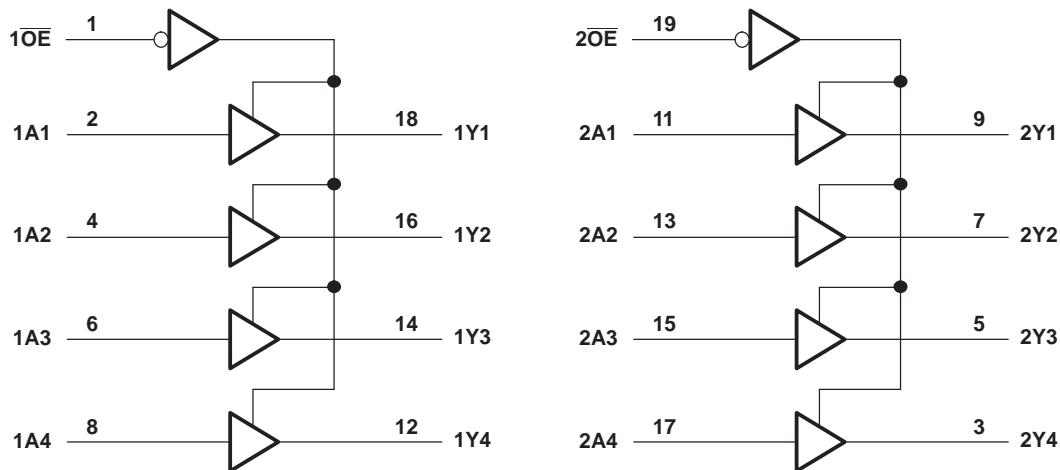
Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6.5	V
V_I	Input voltage range[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2][3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance	DB package[4]		70	°C/W
		DBQ package[4]		68	
		DGV package[4]		92	
		DW package[4]		58	
		NS package[4]		60	
		PW package[4]		83	
		RGY package[5]		37	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) The package thermal impedance is calculated in accordance with JESD 51-5.

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Recommended Operating Conditions[1]

			SN54LVCH244A MIN	SN54LVCH244A MAX	SN74LVCH244A MIN	SN74LVCH244A MAX	UNIT
V_{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V			$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V			1.7		
		V_{CC} = 2.7 V to 3.6 V	2		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V				$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V				0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V				−4	mA
		V_{CC} = 2.3 V				−8	
		V_{CC} = 2.7 V		−12		−12	
		V_{CC} = 3 V		−24		−24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V				4	mA
		V_{CC} = 2.3 V				8	
		V_{CC} = 2.7 V		12		12	
		V_{CC} = 3 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	SN54LVCH244A MIN	TYP[1]	MAX	SN74LVCH244A MIN	TYP[1]	MAX	UNIT
V_{OH}	$I_{OH} = -100$ µA		1.65 V to 3.6 V				$V_{CC} - 0.2$			V
			2.7 V to 3.6 V	$V_{CC} - 0.2$						
	$I_{OH} = -4$ mA		1.65 V				1.2			
	$I_{OH} = -8$ mA		2.3 V				1.7			
	$I_{OH} = -12$ mA		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	$I_{OH} = -24$ mA		3 V	2.2			2.2			
V_{OL}	$I_{OL} = 100$ µA		1.65 V to 3.6 V						0.2	V
			2.7 V to 3.6 V			0.2				
	$I_{OL} = 4$ mA		1.65 V						0.45	
	$I_{OL} = 8$ mA		2.3 V						0.7	
	$I_{OL} = 12$ mA		2.7 V			0.4			0.4	
	$I_{OL} = 24$ mA		3 V			0.55			0.55	
I_I	$V_I = 0$ to 5.5 V		3.6 V			±5			±5	µA
I_{off}	V_I or $V_O = 5.5$ V		0						±10	µA
$I_{I(hold)}$	$V_I = 0.58$ V		1.65 V				(2)			µA
	$V_I = 1.07$ V						(2)			
	$V_I = 0.7$ V		2.3 V				45			
	$V_I = 1.7$ V						−45			
	$V_I = 0.8$ V		3 V	75			75			
	$V_I = 2$ V			−75			−75			
	$V_I = 0$ to 3.6 V[3]		3..6 V			±500			±500	
I_{OZ}	$V_O = 0$ to 5.5 V		3.6 V			±15			±10	µA
I_{CC}	$V_I = V_{CC}$ or GND	$I_O = 0$	3.6 V			10			10	µA
	3.6 V $\leq V_I \leq 5.5$ V[4]					10			10	
ΔI_{CC}	One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V		4	12		4		pF
C_o	$V_O = V_{CC}$ or GND		3.3 V		5.5	12		5.5		pF

(1) All typical values are at $V_{CC} = 3.3$ V, $T_A = 25°C$.
(2) This information was not available at the time of publication.
(3) This is the bus-hold maximum dynamic current required to switch the input from one state to another.
(4) This applies in the disabled state only.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVCH244A				UNIT
			V_{CC} = 2.7 V		V_{CC} = 3.3 V $\pm$ 0.3 V		
			MIN	MAX	MIN	MAX	
t_{pd}	A	Y		7.5	1	6.5	ns
t_{en}	$\overline{OE}$	Y		9	1	8	ns
t_{dis}	$\overline{OE}$	Y		8	1	7	ns

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVCH244A								UNIT
			V_{CC} = 1.8 V $\pm$ 0.15 V		V_{CC} = 2.5 V $\pm$ 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V $\pm$ 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	(1)	(1)	(1)	(1)		6.9	1.5	5.9	ns
t_{en}	$\overline{OE}$	Y	(1)	(1)	(1)	(1)		8.6	1	7.6	ns
t_{dis}	$\overline{OE}$	Y	(1)	(1)	(1)	(1)		6.8	1.5	5.8	ns

(1)   This information was not available at the time of publication.

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	(1)	(1)	47	pF
	Outputs disabled		(1)	(1)	2	

(1)   This information was not available at the time of publication.

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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

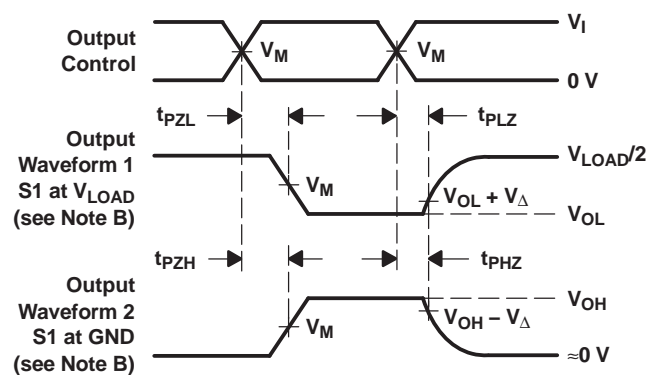| V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
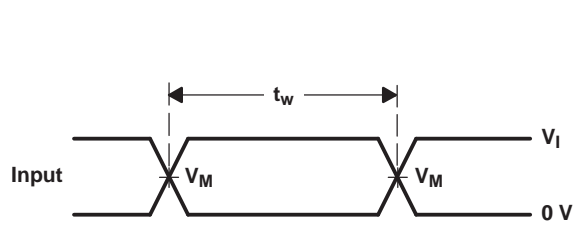
VOLTAGE WAVEFORMS
PULSE DURATION
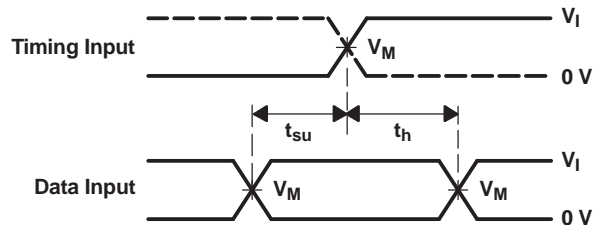
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
   D. The outputs are measured one at a time, with one transition per measurement.
   E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
   F. t_{PZL} and t_{PZH} are the same as t_{en}.
   G. t_{PLH} and t_{PHL} are the same as t_{pd}.
   H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9754201Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9754201Q2A SNJ54LVCH 244AFK	Samples
5962-9754201QRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9754201QR A SNJ54LVCH244AJ	Samples
5962-9754201QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9754201QS A SNJ54LVCH244AW	Samples
5962-9754201V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9754201V2A SNV54LVCH 244AFK	Samples
5962-9754201VRA	ACTIVE	CDIP	J	20	20	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9754201VR A SNV54LVCH244AJ	Samples
5962-9754201VSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9754201VS A SNV54LVCH244AW	Samples
SN74LVCH244ADBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 85		
SN74LVCH244ADBQR	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVCH244A	Samples
SN74LVCH244ADBQRE4	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVCH244A	Samples
SN74LVCH244ADBQRG4	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVCH244A	Samples
SN74LVCH244ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A	Samples
SN74LVCH244ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A	Samples
SN74LVCH244ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A	Samples
SN74LVCH244ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCH244ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A	Samples
SN74LVCH244ADGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A	Samples
SN74LVCH244ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A	Samples
SN74LVCH244ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A	Samples
SN74LVCH244ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A	Samples
SN74LVCH244ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A	Samples
SN74LVCH244ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A	Samples
SN74LVCH244ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A	Samples
SN74LVCH244ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A	Samples
SN74LVCH244ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A	Samples
SN74LVCH244ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH244A	Samples
SN74LVCH244APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A	Samples
SN74LVCH244APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A	Samples
SN74LVCH244APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A	Samples
SN74LVCH244APWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
SN74LVCH244APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A	Samples
SN74LVCH244APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A	Samples
SN74LVCH244APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCH244APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A	Samples
SN74LVCH244APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A	Samples
SN74LVCH244APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH244A	Samples
SN74LVCH244ARGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LCH244A	Samples
SN74LVCH244ARGYRG4	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LCH244A	Samples
SNJ54LVCH244AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9754201Q2A SNJ54LVCH 244AFK	Samples
SNJ54LVCH244AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9754201QR A SNJ54LVCH244AJ	Samples
SNJ54LVCH244AW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9754201QS A SNJ54LVCH244AW	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVCH244A, SN54LVCH244A-SP, SN74LVCH244A :

- Catalog: SN74LVCH244A, SN54LVCH244A

- Automotive: SN74LVCH244A-Q1, SN74LVCH244A-Q1

- Military: SN54LVCH244A

- Space: SN54LVCH244A-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCH244ADBQR	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVCH244ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVCH244ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVCH244ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LVCH244ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LVCH244APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVCH244APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVCH244ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCH244ADBQR	SSOP	DBQ	20	2500	367.0	367.0	38.0
SN74LVCH244ADBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LVCH244ADGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74LVCH244ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVCH244ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LVCH244APWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74LVCH244APWT	TSSOP	PW	20	250	367.0	367.0	38.0
SN74LVCH244ARGYR	VQFN	RGY	20	3000	367.0	367.0	35.0

PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	───	───	───	───
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
    B. This drawing is subject to change without notice.
    C. This package is hermetically sealed with a ceramic lid using glass frit.
    D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
    E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

W (R–GDFP–F20)   **CERAMIC DUAL FLATPACK**

Base and Seating Plane

0.300 (7,62) / 0.245 (6,22)

0.045 (1,14) / 0.026 (0,66)

0.009 (0,23) / 0.004 (0,10)

0.100 (2,45) / 0.045 (1,14)

0.320 (8,13) MAX

0.540 (13,72) MAX

0.022 (0,56) / 0.015 (0,38)

0.050 (1,27)

0.005 (0,13) MIN
4 Places

0.370 (9,40) / 0.250 (6,35)

0.370 (9,40) / 0.250 (6,35)

1   20

10   11
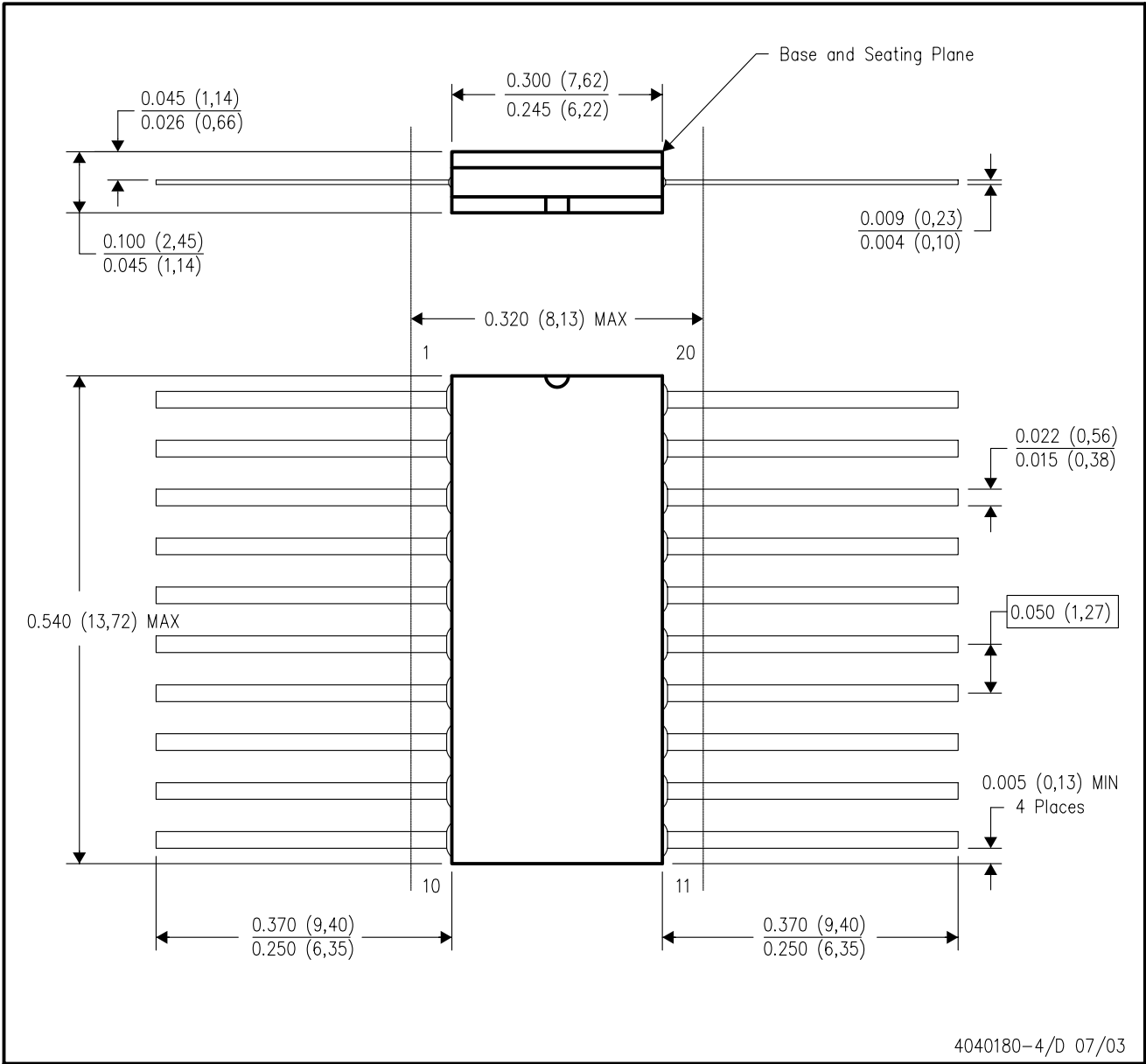
4040180–4/D 07/03

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   This package can be hermetically sealed with a ceramic lid using glass frit.
          D.   Index point is provided on cap for terminal identification only.
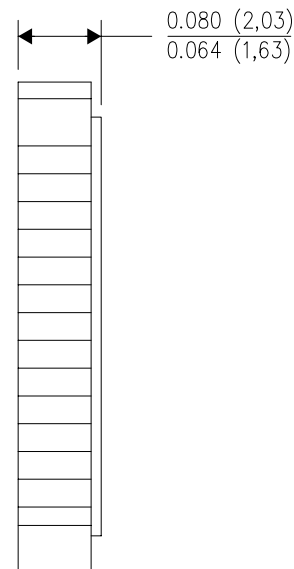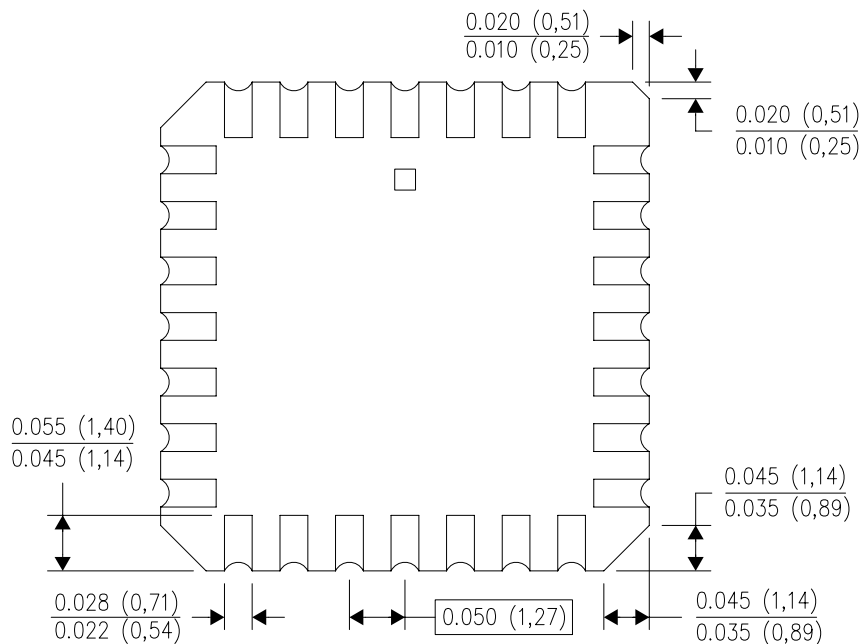   E.   Falls within Mil–Std 1835 GDFP2–F20

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FK (S−CQCC−N**)
28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

B SQ

A SQ

$\frac{0.020\ (0,51)}{0.010\ (0,25)}$

$\frac{0.020\ (0,51)}{0.010\ (0,25)}$

$\frac{0.080\ (2,03)}{0.064\ (1,63)}$

$\frac{0.055\ (1,40)}{0.045\ (1,14)}$

$\frac{0.045\ (1,14)}{0.035\ (0,89)}$

$\frac{0.028\ (0,71)}{0.022\ (0,54)}$

0.050 (1,27)

$\frac{0.045\ (1,14)}{0.035\ (0,89)}$

4040140/D 01/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a metal lid.
         D.   Falls within JEDEC MS−004

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DGV (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

0,40   0,23 / 0,13   ⊕ | 0,07 Ⓜ

24   13

4,50 / 4,30   6,60 / 6,20

1   12

A

0,16 NOM

Gage Plane

0°–8°

0,25

0,75 / 0,50

1,20 MAX

0,15 / 0,05

Seating Plane   ◠ | 0,08

DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
    B. This drawing is subject to change without notice.
    C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
    D. Falls within JEDEC: 24/48 Pins – MO-153
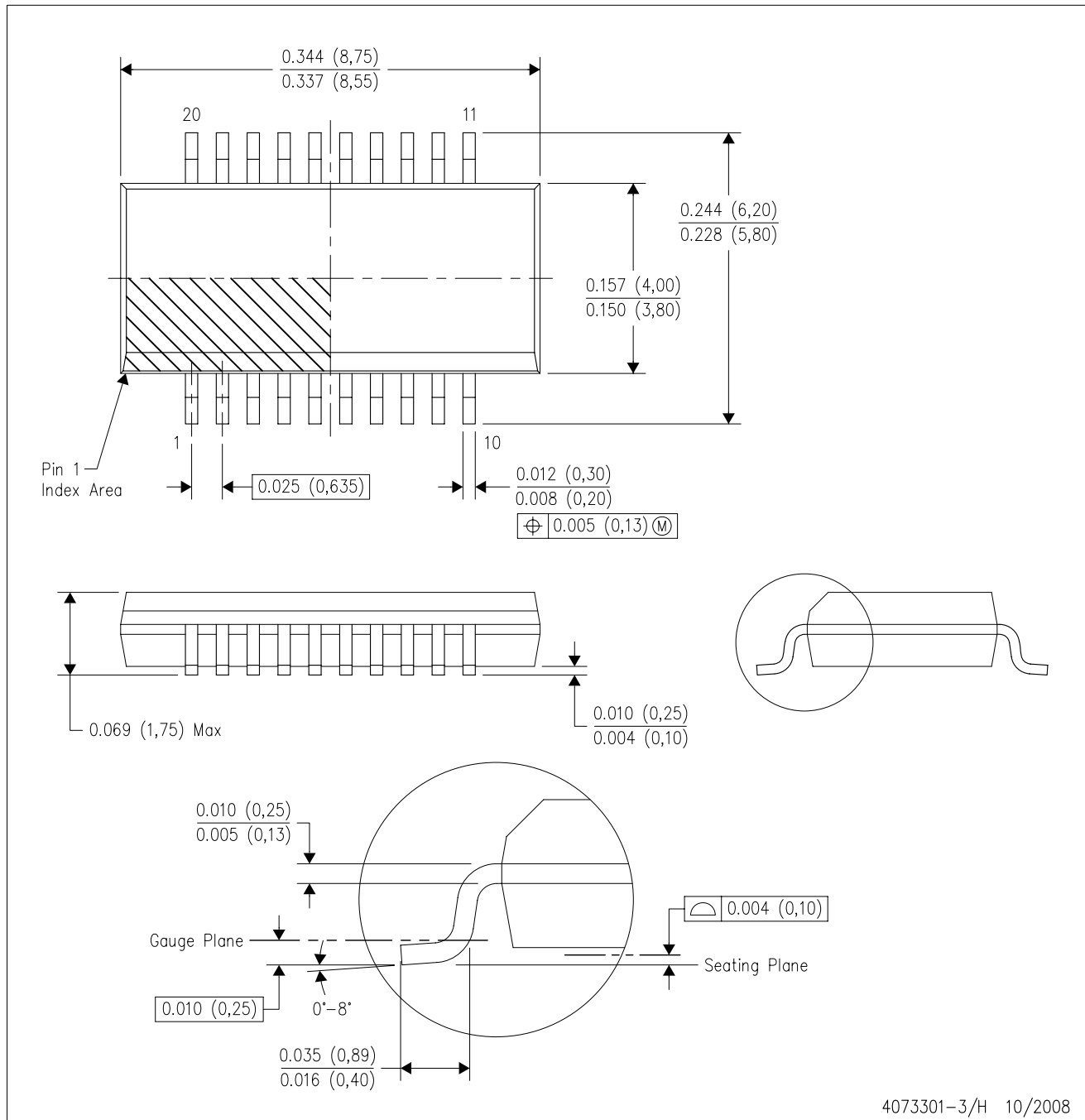   14/16/20/56 Pins – MO-194

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0.512 (13,00)
0.496 (12,60)

20   11

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−4/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
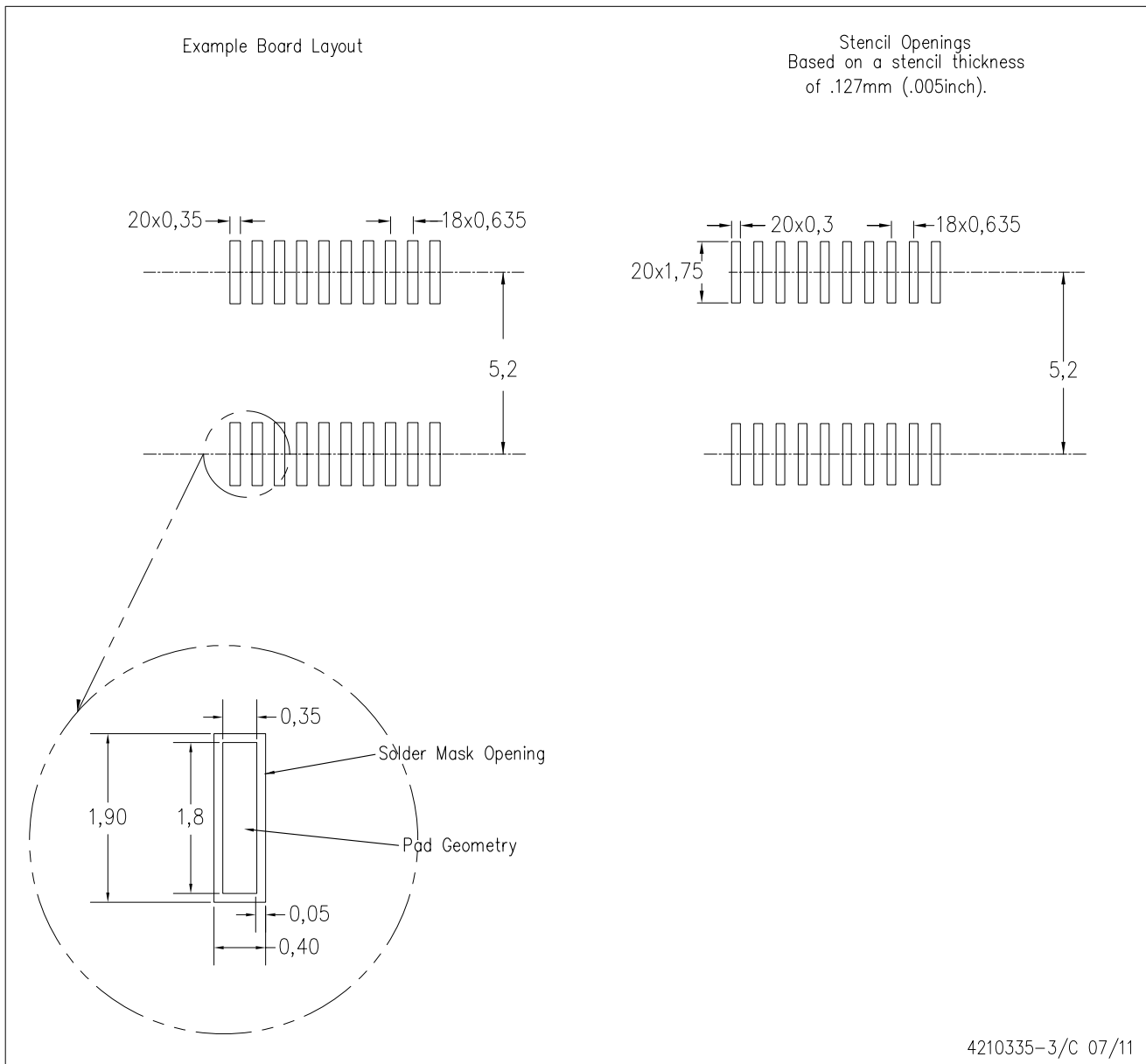   D.   Falls within JEDEC MS−013 variation AC.

DBQ (R−PDSO−G20)   PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

20   11

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1   10

Pin 1
Index Area

0.025 (0,635)

0.012 (0,30)
0.008 (0,20)

⊕ | 0.005 (0,13) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)   0°−8°

0.035 (0,89)
0.016 (0,40)

4073301−3/H   10/2008

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
         D.   Falls within JEDEC MO−137 variation AD.

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DBQ (R−PDSO−G20)   PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

20x0,35 →| |←   →| |←18x0,635

5,2

→| |← 20x0,3   → →| |←18x0,635

20x1,75

5,2

←0,35

Solder Mask Opening

1,90   1,8

Pad Geometry

←0,05

0,40

4210335−3/C 07/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D.   Publication IPC−7351 is recommended for alternate designs.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
              metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

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PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0,65
0,30 / 0,19
⊕ 0,10 Ⓜ

20   11

4,50 / 4,30   6,60 / 6,20

Ⓓ

1   10

6,60 / 6,40

Ⓒ

0,15 NOM

Gage Plane

0°−8°

0,25

0,75 / 0,50

1,20 MAX

0,15 / 0,05

Seating Plane

⌒ 0,10

4040064−5/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
           B.   This drawing is subject to change without notice.
           Ⓒ   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
                not exceed 0,15 each side.
           Ⓓ   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
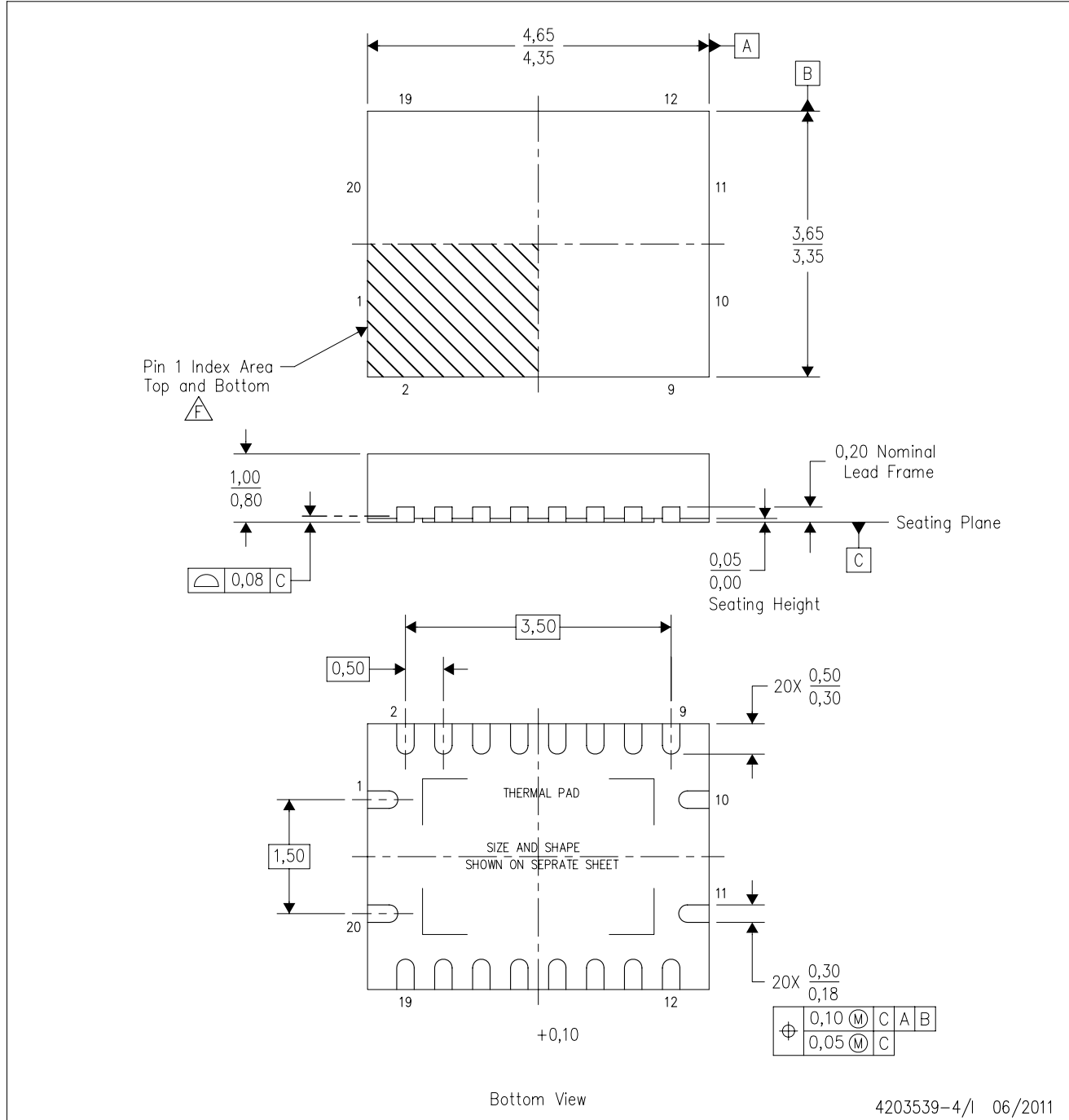   E.   Falls within JEDEC MO−153

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PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

1,55

5,6

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)

0,3

Pad Geometry

1,6

0,07
All Around

4211284−5/F   12/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate design.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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RGY (R–PVQFN–N20)   PLASTIC QUAD FLATPACK NO–LEAD

4,65 / 4,35 [A]

[B]

19   12

20   11

3,65 / 3,35

1   10

2   9

Pin 1 Index Area
Top and Bottom
[F]

1,00 / 0,80

0,20 Nominal
Lead Frame

Seating Plane

[C]

⌒ | 0,08 | C

0,05 / 0,00
Seating Height

3,50

0,50

20X 0,50 / 0,30

2   9

1   10

THERMAL PAD

1,50

SIZE AND SHAPE
SHOWN ON SEPRATE SHEET

20   11

19   12

+0,10

20X 0,30 / 0,18

⊕ | 0,10 ⓜ | C | A | B
    | 0,05 ⓜ | C

Bottom View

4203539–4/I   06/2011

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M–1994.
         B.   This drawing is subject to change without notice.
         C.   QFN (Quad Flatpack No–Lead) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
   [F]   Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
         The Pin 1 identifiers are either a molded, marked, or metal feature.
         G.   Package complies to JEDEC MO–241 variation BA.
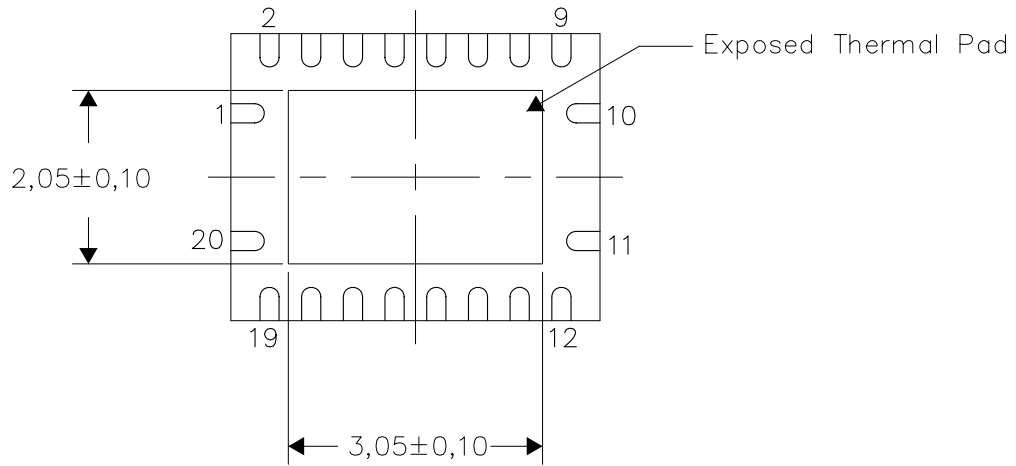
RGY (R−PVQFN−N20)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

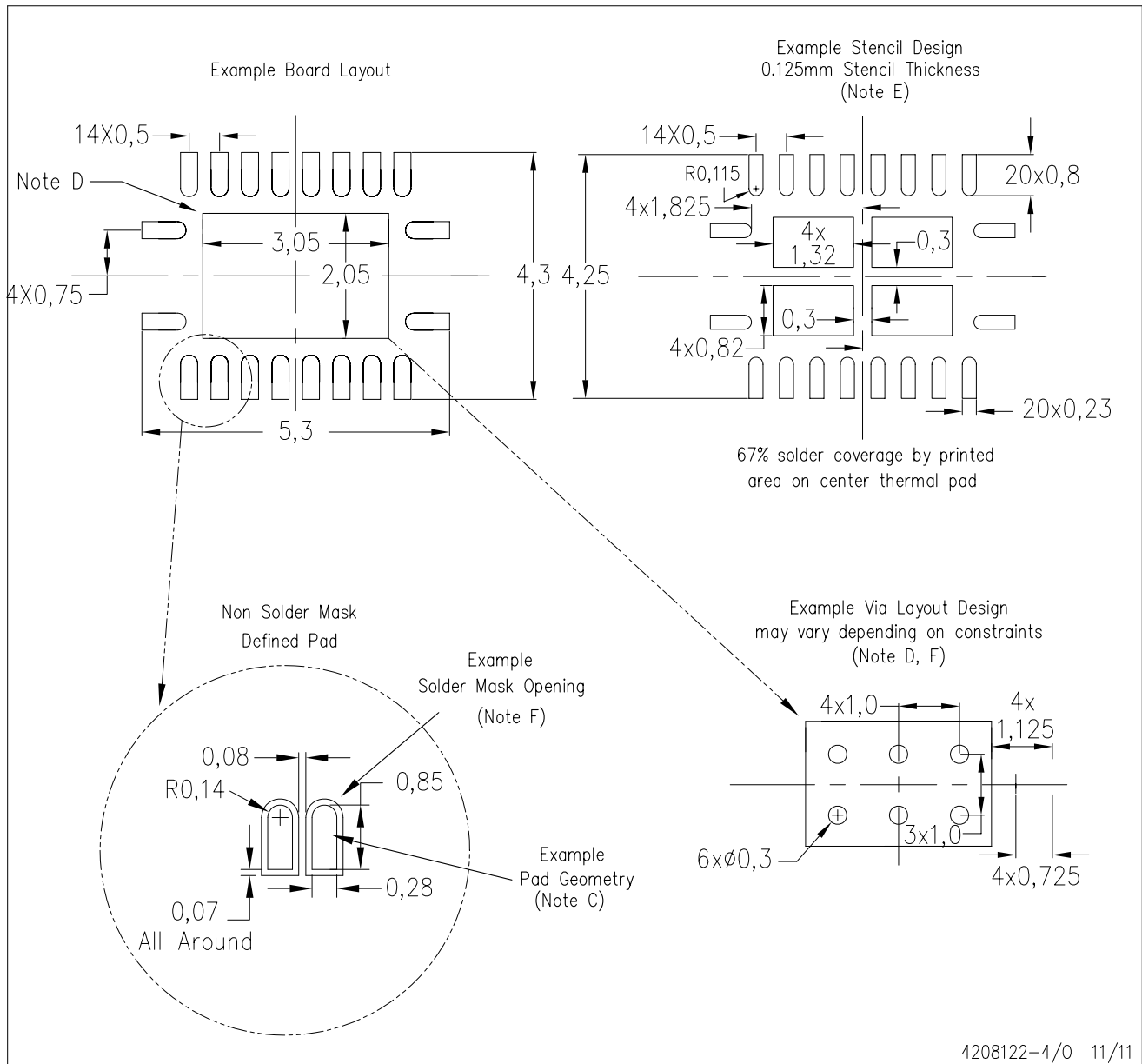The exposed thermal pad dimensions for this package are shown in the following illustration.

Exposed Thermal Pad

2,05±0,10

3,05±0,10

Bottom View

Exposed Thermal Pad Dimensions

4206353−4/O   11/11

NOTE: All linear dimensions are in millimeters

RGY (R−PVQFN−N20)　　　　　PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

14X0,5

Note D

4X0,75

3,05

2,05

4,3 4,25

5,3

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

14X0,5

R0,115

4x1,825

20x0,8

4x
1,32

0,3

0,3

4x0,82

20x0,23

67% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,07

0,28

All Around

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

4x1,0

4x
1,125

6xØ0,3

3x1,0

4x0,725

4208122−4/0 11/11

NOTES:　A.　All linear dimensions are in millimeters.
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　Publication IPC−7351 is recommended for alternate designs.
　　　　　D.　This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
　　　　　　　QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
　　　　　　　for specific thermal information, via requirements, and recommended board layout.
　　　　　　　These documents are available at www.ti.com <http://www.ti.com>.
　　　　　E.　Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
　　　　　　　contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
　　　　　F.　Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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NS (R-PDSO-G)**   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

	PINS **	14	16	20	24
DIM					
A	MAX	10,50	10,50	12,90	15,30
A	MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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