

SN5407, SN5417, SN7407, SN7417 HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

SDLS032G – DECEMBER 1983 – REVISED MAY 2004

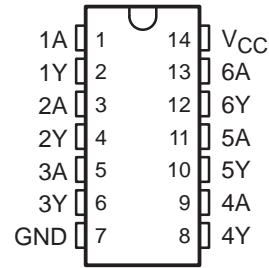
- Convert TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Driver for Indicator Lamps and Relays
- Inputs Fully Compatible With Most TTL Circuits

description/ordering information

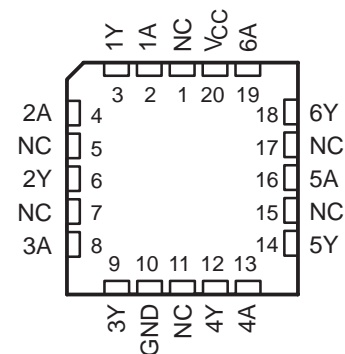
These TTL hex buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS) or for driving high-current loads (such as lamps or relays) and also are characterized for use as buffers for driving TTL inputs. The SN5407 and SN7407 have minimum breakdown voltages of 30 V, and the SN5417 and SN7417 have minimum breakdown voltages of 15 V. The maximum sink current is 30 mA for the SN5407 and SN5417 and 40 mA for the SN7407 and SN7417.

These devices perform the Boolean function $Y = A$ in positive logic.

SN5407, SN5417 . . . J OR W PACKAGE
SN7407, SN7417 . . . D, N, OR NS PACKAGE
(TOP VIEW)



SN5407 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

| T _A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING | |
|----------------|---------------|---------------|-----------------------|------------------|---------|
| 0°C to 70°C | SOIC – D | Tube | SN7407D | 7407 | |
| | | Tape and reel | SN7407DR | | |
| | | Tube | SN7417D | 7417 | |
| | | Tape and reel | SN7417DR | | |
| | PDIP – N | Tube | | SN7407N | SN7407N |
| | | | | SN7417N | SN7417N |
| SOP – NS | Tape and reel | | SN7407NSR | SN7407 | |
| | | | SN7417NSR | SN7417 | |
| –55°C to 125°C | CDIP – J | Tube | SNJ5407J | SNJ5407J | |
| | | | SNJ5417J | SNJ5417J | |
| | CFP – W | Tube | SNJ5407W | SNJ5407W | |
| | LCCC – FK | Tube | SNJ5407FK | SNJ5407FK | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN5407, SN5417, SN7407, SN7417 HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

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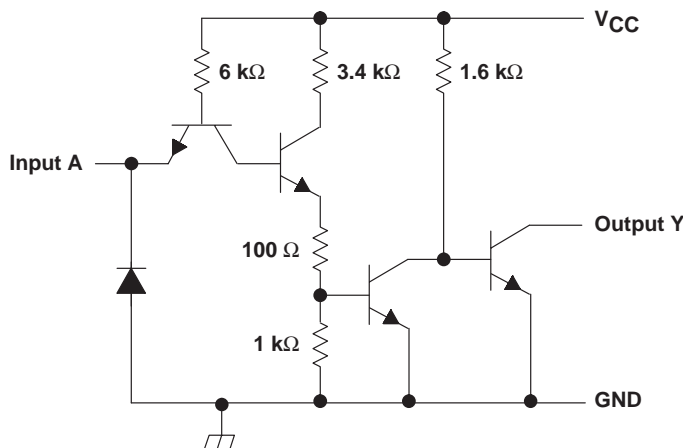
description/ordering information (continued)

These circuits are completely compatible with most TTL families. Inputs are diode clamped to minimize transmission-line effects, which simplifies design. Typical power dissipation is 145 mW, and average propagation delay time is 14 ns.

logic diagram, each buffer/driver (positive logic)



schematic



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I (see Note 1) | 5.5 V |
| Output voltage, V_O (see Notes 1 and 2): SN5407, SN7407 | 30 V |
| SN5417, SN7417 | 15 V |
| Package thermal impedance, θ_{JA} (see Note 3): D package | 86°C/W |
| N package | 80°C/W |
| NS package | 76°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to GND.
 2. This is the maximum voltage that should be applied to any output when it is in the off state.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.



SN5407, SN5417, SN7407, SN7417 HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

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recommended operating conditions (see Note 4)

| | | MIN | NOM | MAX | UNIT | | |
|-----------------|--------------------------------|----------------|------|-----|------|-----|----|
| V _{CC} | Supply voltage | SN5407, SN5417 | 4.5 | 5 | 5.5 | V | |
| | | SN7407, SN7417 | 4.75 | 5 | 5.25 | | |
| V _{IH} | High-level input voltage | 2 | | | V | | |
| V _{IL} | Low-level input voltage | | | | 0.8 | V | |
| V _{OH} | High-level output voltage | SN5407, SN7407 | | | 30 | V | |
| | | SN5417, SN7417 | | | 15 | | |
| I _{OL} | Low-level output current | SN5407, SN5417 | | | 30 | mA | |
| | | SN7407, SN7417 | | | 40 | | |
| T _A | Operating free-air temperature | SN5407, SN5417 | -55 | | | 125 | °C |
| | | SN7407, SN7417 | 0 | | | 70 | |

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | | MIN | TYP‡ | MAX | UNIT | |
|------------------|------------------------|-------------------------|--|------|------|------|----|
| V _{IK} | V _{CC} = MIN, | I _I = -12 mA | | | -1.5 | V | |
| I _{OH} | V _{CC} = MIN, | V _{IH} = 2 V | V _{OH} = 30 V (SN5407, SN7407) | | 0.25 | mA | |
| | | | V _{OH} = 15 V (SN5417, SN7417) | | 0.25 | | |
| V _{OL} | V _{CC} = MIN, | V _{IL} = 0.8 V | I _{OL} = 16 mA | | 0.4 | V | |
| | | | I _{OL} = 30 mA (SN5407, SN5417) | | 0.7 | | |
| | | | I _{OL} = 40 mA (SN7407, SN7417) | | 0.7 | | |
| I _I | V _{CC} = MAX, | V _I = 5.5 V | | | 1 | mA | |
| I _{IH} | V _{CC} = MAX, | V _{IH} = 2.4 V | | | 40 | μA | |
| I _{IL} | V _{CC} = MAX, | V _{IL} = 0.4 V | | | -1.6 | mA | |
| I _{CCH} | V _{CC} = MAX | | | | 29 | 41 | mA |
| I _{CCL} | V _{CC} = MAX | | | | 21 | 30 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

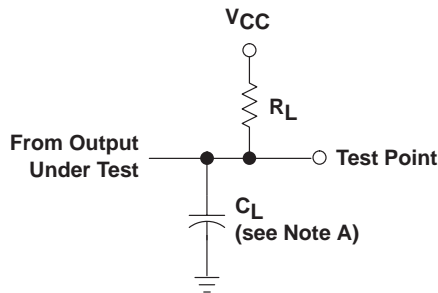
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--------------|-------------|--|-----|-----|-----|------|
| t _{PLH} | A | Y | R _L = 110 Ω, C _L = 15 pF | 6 | 10 | 10 | ns |
| t _{PHL} | | | | 20 | 30 | | |
| t _{PLH} | A | Y | R _L = 150 Ω, C _L = 50 pF | | | 15 | ns |
| t _{PHL} | | | | | | 26 | |

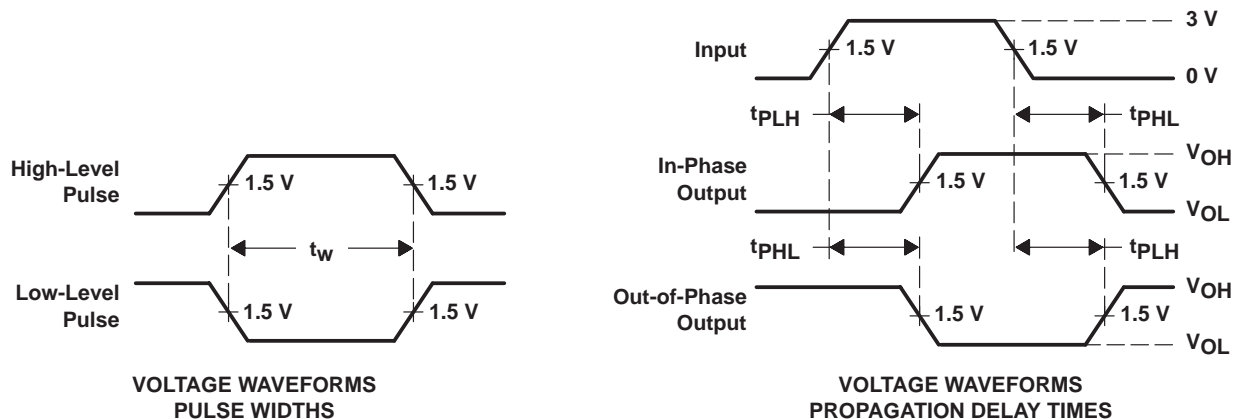
SN5407, SN5417, SN7407, SN7417
HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



- NOTES: A. C_L includes probe and jig capacitance.
 B. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 7$ ns, $t_f \leq 7$ ns.
 D. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| JM38510/00803BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 00803BCA | Samples |
| JM38510/00803BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 00803BDA | Samples |
| M38510/00803BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 00803BCA | Samples |
| M38510/00803BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 00803BDA | Samples |
| SN5407J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN5407J | Samples |
| SN5417J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN5417J | Samples |
| SN7407D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7407 | Samples |
| SN7407DE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7407 | Samples |
| SN7407DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7407 | Samples |
| SN7407DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7407 | Samples |
| SN7407DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7407 | Samples |
| SN7407DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7407 | Samples |
| SN7407J | OBSOLETE | CDIP | J | 14 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN7407N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN7407N | Samples |
| SN7407N3 | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN7407NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN7407N | Samples |
| SN7407NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN7407 | Samples |
| SN7407NSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN7407 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| SN7407NSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN7407 | Samples |
| SN7417D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7417 | Samples |
| SN7417DE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7417 | Samples |
| SN7417DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7417 | Samples |
| SN7417DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7417 | Samples |
| SN7417DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7417 | Samples |
| SN7417DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7417 | Samples |
| SN7417N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN7417N | Samples |
| SN7417N3 | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN7417NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN7417N | Samples |
| SNJ5407FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ5407FK | Samples |
| SNJ5407J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ5407J | Samples |
| SNJ5407W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ5407W | Samples |
| SNJ5417J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ5417J | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN5407, SN5417, SN7407, SN7417 :

● Catalog: [SN7407](#), [SN7417](#)

● Military: [SN5407](#), [SN5417](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN7407DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.55 | 9.05 | 2.1 | 8.0 | 16.0 | Q1 |
| SN7407DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN7407NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN7417DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN7407DR | SOIC | D | 14 | 2500 | 385.0 | 388.0 | 194.0 |
| SN7407DR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN7407NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN7417DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

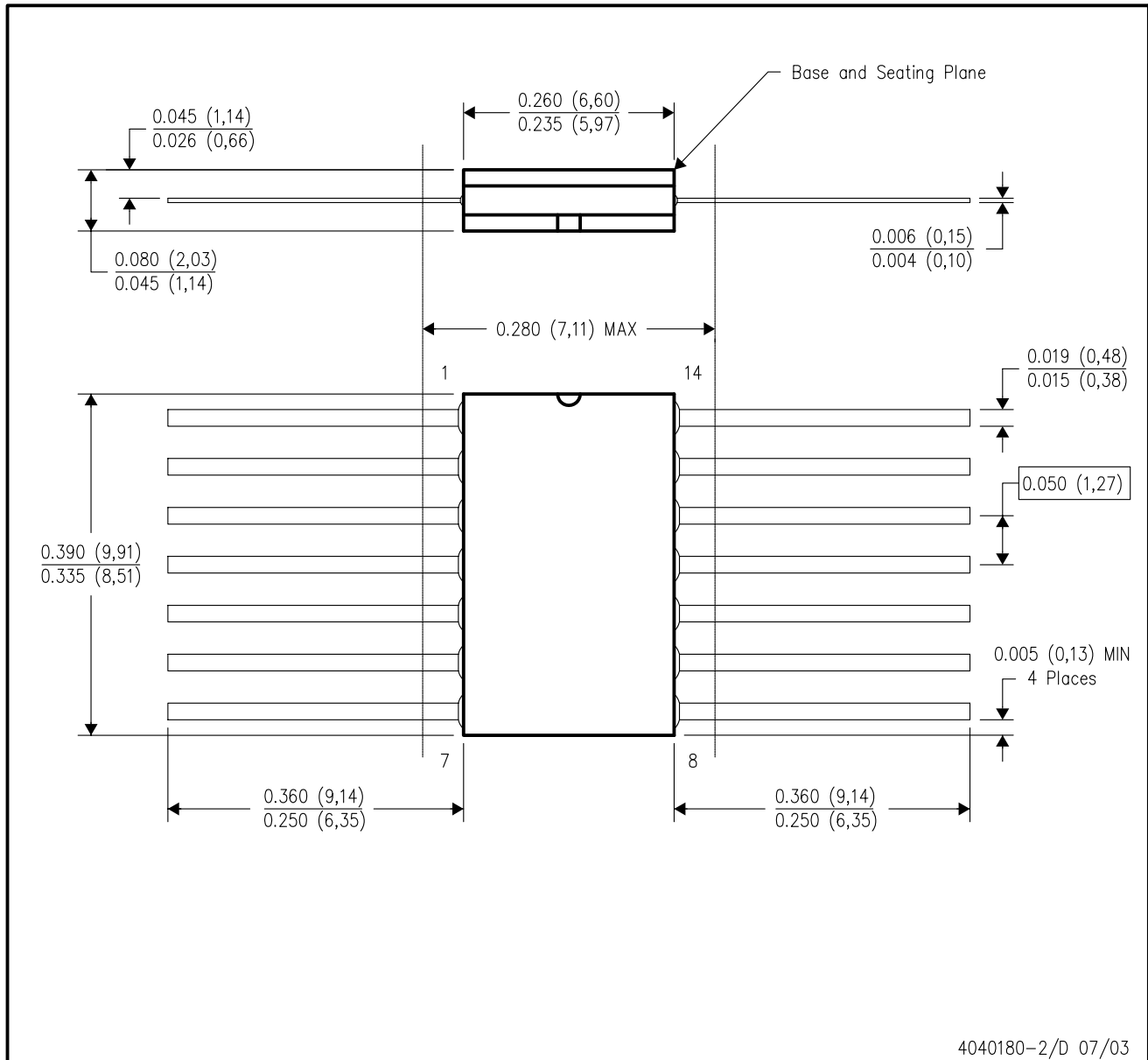


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/D 07/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

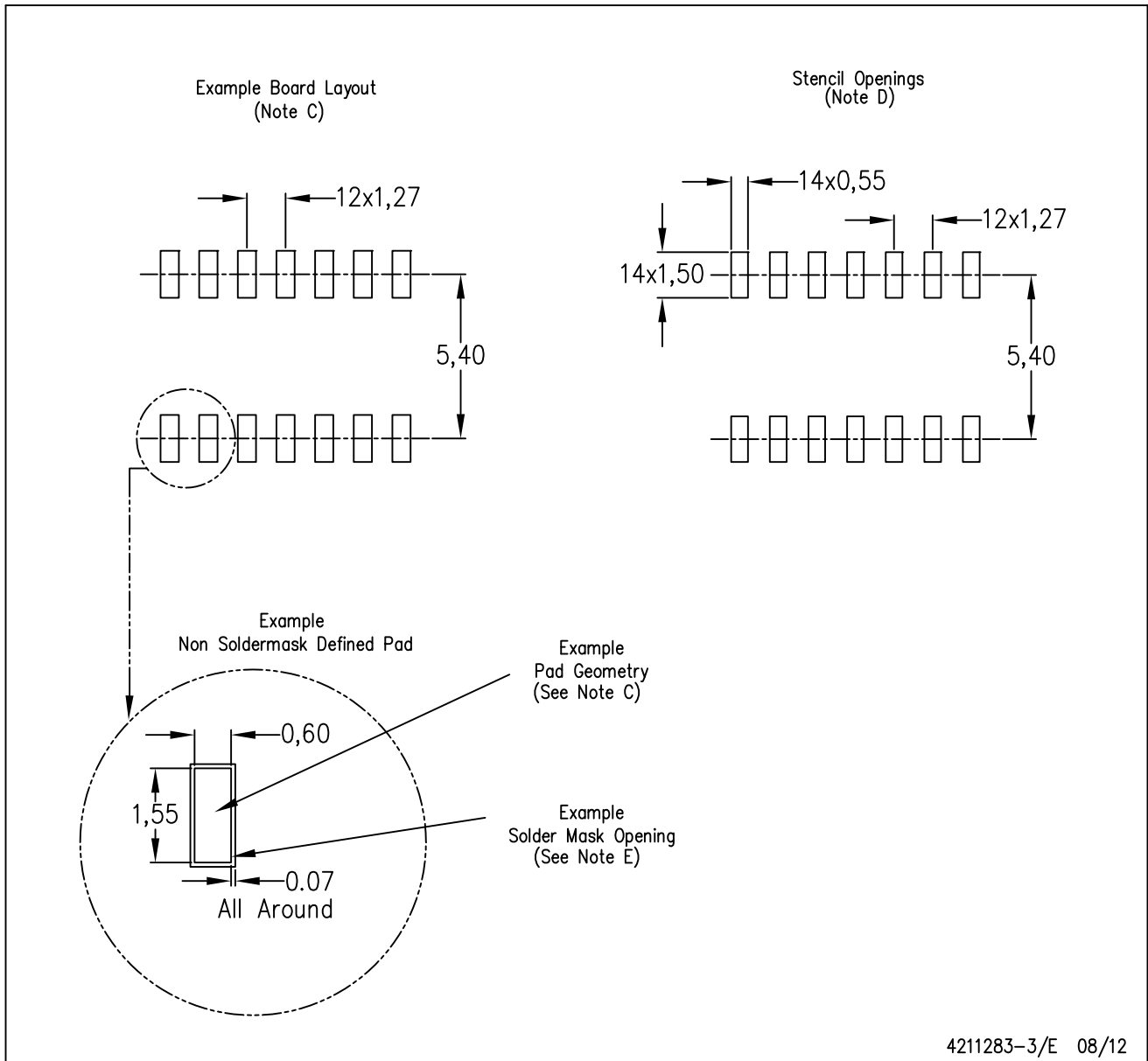
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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