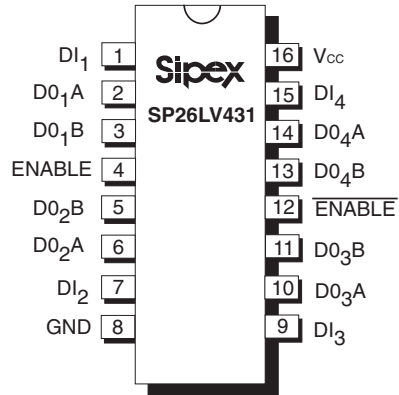# High Speed, +3.3V Quad RS-422 Differential Line Driver

## FEATURES

- Quad Differential Line Drivers
- Compatible with the EIA standard for RS-422 serial protocol
- High-Z Output Control
- At Least 60Mbps Transmission Rates
- 11ns Typical Driver Propagation Delays
- Less than 1ns Typical Output Skew
- Single +3.3V Supply Operation
- Common Driver Enable Control
- Compatibility with the industry standard 26LV31
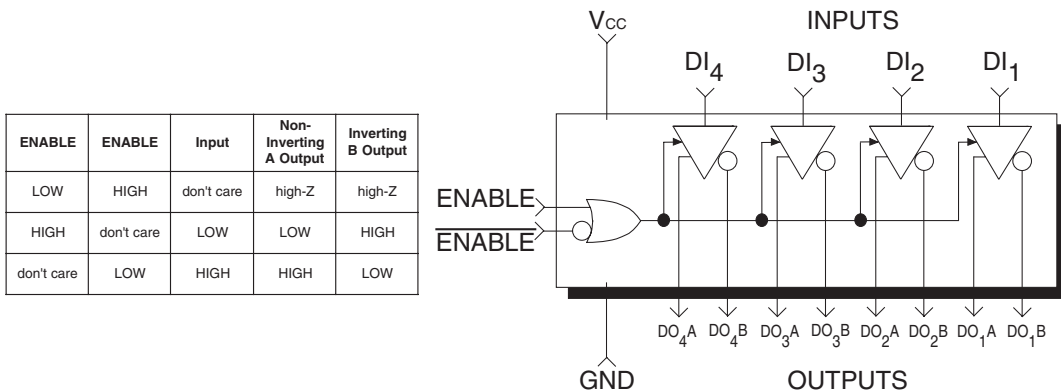- Ideal For Use with SP26LV431, Quad Receivers

```
          ┌────── ⌴ ──────┐
DI₁   1   │    Sipex       │  16   Vcc
DO₁A  2   │   SP26LV431    │  15   DI₄
DO₁B  3   │                │  14   DO₄A
ENABLE 4  │                │  13   DO₄B
DO₂B  5   │                │  12   ENABLE
DO₂A  6   │                │  11   DO₃B
DI₂   7   │                │  10   DO₃A
GND   8   │                │  9    DI₃
          └────────────────┘
```

Pin assignments:

$DI_1$ — 1, $V_{CC}$ — 16
$DO_1A$ — 2, $DI_4$ — 15
$DO_1B$ — 3, $DO_4A$ — 14
ENABLE — 4, $DO_4B$ — 13
$DO_2B$ — 5, $\overline{ENABLE}$ — 12
$DO_2A$ — 6, $DO_3B$ — 11
$DI_2$ — 7, $DO_3A$ — 10
GND — 8, $DI_3$ — 9

*Now Available in Lead Free Packaging*

## DESCRIPTION

The **SP26LV431** is a quad differential line driver that meets the specifications of the EIA standard RS-422 serial protocol. The **SP26LV431** features Sipex's BiCMOS process allowing low power operational characteristics of CMOS technology while meeting all of the demands of the RS-422 serial protocol over 60Mbps under load. The RS-422 protocol allows up to 10 receivers to be connected to a multipoint bus transmission line. The **SP26LV431** features a driver enable control common to all four drivers that places the output pins in a high impedance state. Since the cabling can be as long as 4,000 feet, the RS-422 drivers of the **SP26LV431** are equipped with a wide common-mode output voltage range to accommodate ground potential differences.

## TYPICAL APPLICATION CIRCUIT

| ENABLE | ENABLE | Input | Non-Inverting A Output | Inverting B Output |
|---|---|---|---|---|
| LOW | HIGH | don't care | high-Z | high-Z |
| HIGH | don't care | LOW | LOW | HIGH |
| don't care | LOW | HIGH | HIGH | LOW |



INPUTS: $DI_4$, $DI_3$, $DI_2$, $DI_1$

ENABLE
$\overline{ENABLE}$

OUTPUTS: $DO_4A$, $DO_4B$, $DO_3A$, $DO_3B$, $DO_2A$, $DO_2B$, $DO_1A$, $DO_1B$

$V_{CC}$ / GND

# ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

$V_{CC}$........................................................................................0.5V to 7.0V
$V_{IN}$ (DC Input Voltage)..............................................-1.5V to ($V_{CC}$ + 1.5V)
$V_{OUT}$ (DC Output Voltage).......................................................-0.5V to 7V
$I_{IK}$, $I_{OK}$ (Clamp Diode Current).........................................................±20mA
$I_{OUT}$ (DC Output Current, per pin)..............................................±150mA
$I_{CC}$ (DC $V_{CC}$ or GND Current, per pin).........................................±150mA
$T_{STG}$ (Storage Temperature Range)...............................-65°C to +150°C
Storage Temperature...................................................-65°C to +150°C

**Power Dissipation Per Package**
16-pin PDIP (derate 14.3mW/°C above +70°C)........................1150mW
16-pin NSOIC (derate 13.6mW/°C above +70°C).....................1100mW

# ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for $V_{CC}$ = +3.0V to +3.6V with $T_{amb}$ = 25°C and all MIN and MAX limits apply across the recommended operating temperature range.

| DC PARAMETERS | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| Supply Voltage, $V_{CC}$ | 3.0 | | 3.6 | V | |
| DC Input or Output Voltage, $V_{IN}$ or $V_{OUT}$ | | | $V_{CC}$ | V | |
| **Input Electrical Characteristics** | | | | | |
| Input Rise or Fall Times, $t_r$ or $t_f$ | | 3 | | ns | |
| HIGH Level Input Voltage, $V_{IH}$ | 2.0 | | | V | |
| LOW Level Input Voltage, $V_{IL}$ | | | 0.8 | V | |
| **Output Electrical Characteristics** | | | | | |
| HIGH Level Output Voltage, $V_{OH}$ | 2.5 | 2.9 | | V | $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OUT}$ = -20mA |
| LOW Level Output Voltage, $V_{OL}$ | | 0.2 | 0.5 | V | $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OUT}$ = 20mA |
| Differential Output Voltage, $V_T$ | 2.0 | 2.7 | | V | $R_L$ = 100Ω, Note 1 |
| Difference in Differential Output, $|V_T| - |\overline{V_T}|$ | | | 0.4 | V | $R_L$ = 100Ω, Note 1 |
| Common Mode Output Voltage, $V_{OS}$ | | | 3.0 | V | $R_L$ = 100Ω, Note 1 |
| Difference in Common Mode Output, $|V_{OS} - \overline{V_{OS}}|$ | | | 0.4 | V | $R_L$ = 100Ω, Note 1 |
| Quiescent Supply Current | | | | | |
| $I_{CC}$ | | | 100 | μA | $V_{IN}$ = $V_{CC}$ or GND, Note 2 |
| Tri-state Output Leakage Current, $I_{OZ}$ | | ±2.0 | | μA | $V_{OUT}$ = $V_{CC}$ or GND, $\overline{ENABLE}$ = $V_{IL}$, $\overline{ENABLE}$ = $V_{IH}$ |
| Output Short Circuit Current, $I_{SC}$ | -30 | | -150 | mA | $V_{IN}$ = $V_{CC}$ or GND, Notes 1 and 3 |
| Output Leakage Current Power Off | | | | | |
| $I_{OFF}$ | | | 100 | μA | $V_{CC}$ = 0V, $V_{OUT}$ = 6V, Note 1 |
| $I_{OFF}$ | | | -100 | μA | $V_{CC}$ = 0V, $V_{OUT}$ = -0.25V, Note 1 |

Unless otherwise noted, the following specifications apply for $V_{CC}$ = +3.0V to +3.6V, $T_{amb}$ = 25°C, $t_r \leq$ 6ns, $t_f \leq$ 6ns, and all MIN and MAX limits apply across the recommended operating temperature range.

| PARAMETERS | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS** | | | | | |
| Propagation Delays, $t_{PLHD}$, $t_{PHLD}$ | | 11 | 18 | ns | Figure 3 |
| Skew | | 0.8 | 2 | ns | Figure 3, Note 4 |
| Differential Ouput Rise and Fall Times, $t_{TLH}$, $t_{PHL}$ | | 4 | 10 | ns | Figure 3 |
| Output Enable Time, $t_{PZH}$ | | | 40 | ns | Figure 5 |
| Output Enable Time, $t_{PZL}$ | | | 40 | ns | Figure 5 |
| Output Disable Time, $t_{PHZ}$ | | | 35 | ns | Figure 5, Note 5 |
| Output Disable Time, $t_{PLZ}$ | | | 35 | ns | Figure 5, Note 5 |
| Power dissipation Capacitance, $C_{PD}$ | | 50 | | pF | Note 6 |
| Input Capacitance, $C_{IN}$ | | 6 | | pF | |

**NOTE 1:** Refer to EIA specifications for RS-422 serial protocol for exact test conditions.
**NOTE 2:** Measured per input. All other inputs at $V_{CC}$ or GND.
**NOTE 3:** This is the current sourced when a high output is shorted to GND. Only one output at a time should be shorted.
**NOTE 4:** Skew is defined as the difference in propagation delays between complementary outputs at the 50% input.
**NOTE 5:** Output disable time is the delay from ENABLE or $\overline{ENABLE}$ being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.
**NOTE 6:** $C_{PD}$ determines the no load dynamic power consumption, $P_D = (C_{PD}V_{CC}^2 f) + (I_{CC}V_{CC})$, and the no load dynamic current consumption, $I_S = (C_{PD}V_{CC}f) + I_{CC}$.
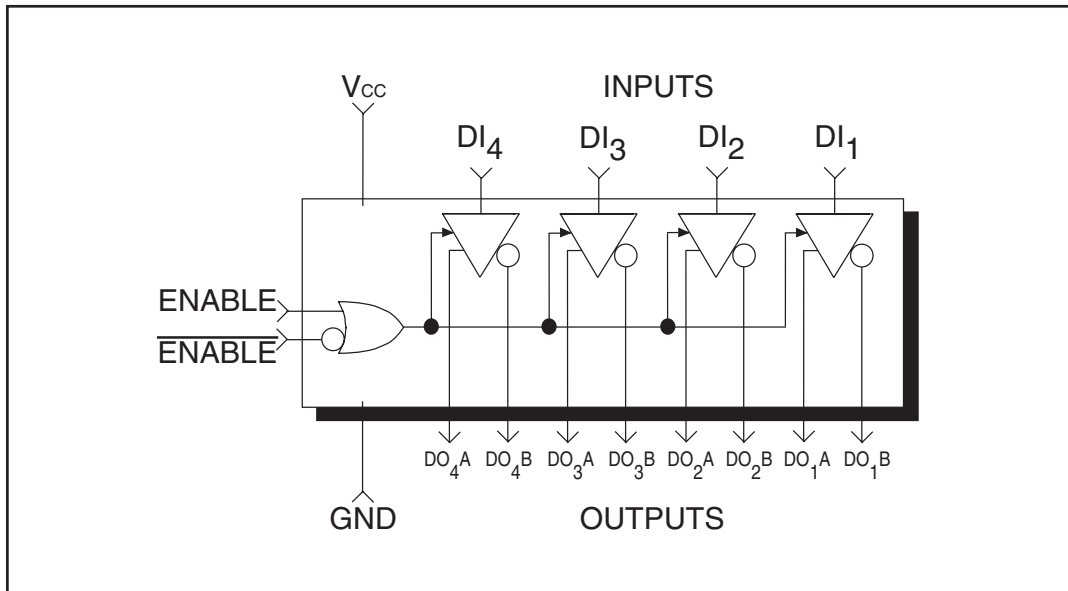


*Figure 1. SP431 Block Diagram*
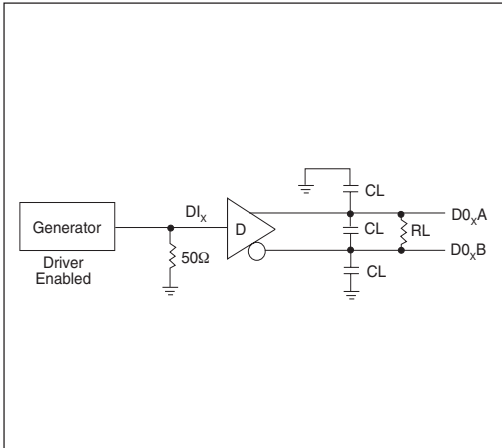
*Figure 2.  AC Test Circuit*
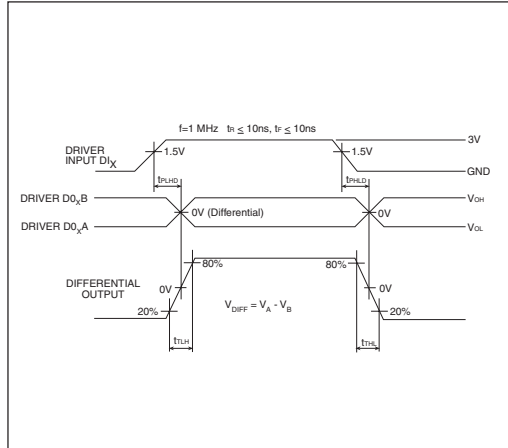


*Figure 3.  Propagation Delays*
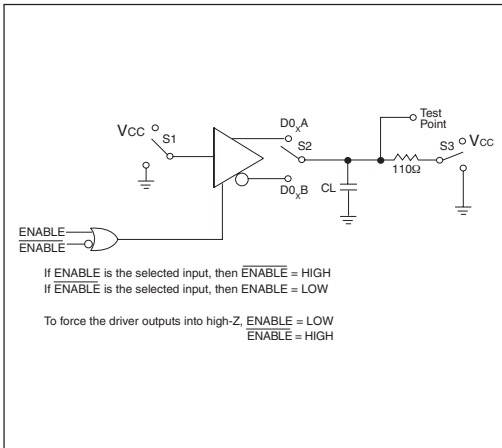


*Figure 4.  Driver Single-Ended TRI-STATE Test Circuit*
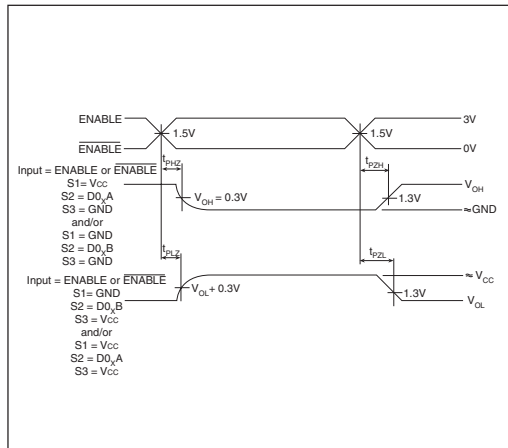


*Figure 5.  Driver Single-Ended TRI-STATE Waveforms*
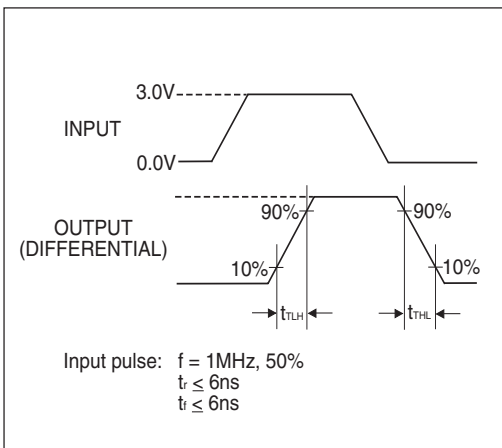


*Figure 6.  Differential Rise and Fall Times*

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The **SP26LV431** is a low-power quad differential line driver designed for digital data transmission meeting the specifications of the EIA standard RS-422 serial protocol. The **SP26LV431** features Sipex's BiCMOS process allowing low power operational characteristics of CMOS technology while meeting all of the demands of the RS-422 serial protocol up to 60Mbps under load in harsh environments.

The RS-422 standard is ideal for multi-drop applications and for long-distance communication. The RS-422 protocol allows up to 10 receivers to be connected to a data bus, making it an ideal choice for multi-drop applications. Since the cabling can be as long as 4,000 feet, RS-422 drivers are equipped with a wide common mode output range to accommodate ground potential differences. Because the RS-422 is a differential interface, data is virtually immune to noise in the transmission line.

The **SP26LV431** accepts TTL or CMOS input levels and translates these to RS-422 output levels. The **SP26LV431** features active HIGH and active LOW driver enable controls common to all four driver channels see *Figure 8*. A logic HIGH on the ENABLE pin (pin 4) or a logic LOW on the ENABLE pin (pin 12) will enable the differential driver outputs. A logic LOW on the ENABLE pin (pin 4) and a logic HIGH on the ENABLE pin (pin 12) will force the driver outputs into high impedance (high-Z). Refer to the truth table in *Figure 8*.

source and sink current capability. All drivers are internally protected against short circuits on their outputs. The driver outputs are short-circuit limited to 150mA. The driver output skew times are typically 0.8ns.

To minimize reflections, the multipoint bus transmission line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible.



*$R_T$ is optional although highly recommended to reduce reflection.

The RS-422 line driver outputs feature high
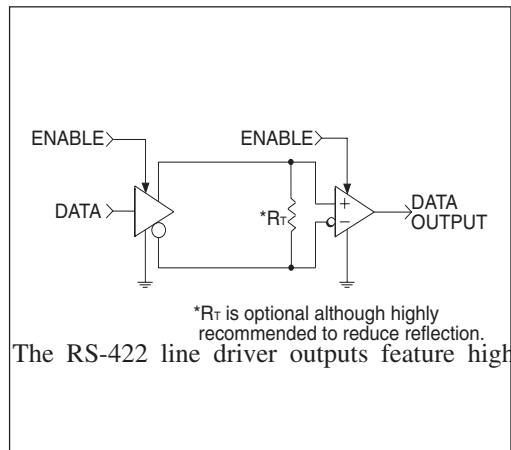
*Figure 7. Two-Wire Balanced System, RS-422*

| ENABLE | ENABLE | Input | Non-Inverting A Output | Inverting B Output |
|---|---|---|---|---|
| LOW | HIGH | don't care | high-Z | high-Z |
| HIGH | don't care | LOW | LOW | HIGH |
| don't care | LOW | HIGH | HIGH | LOW |

*Figure 8. Truth Table, Enable / Disable Function Common to All Four RS-422 Drivers*
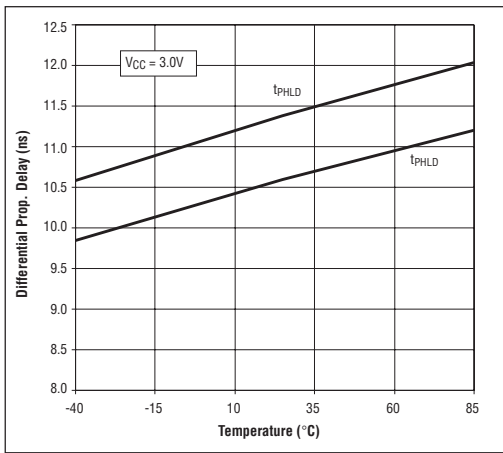
*Figure 9. Differential Propagation Delay vs Temperature*
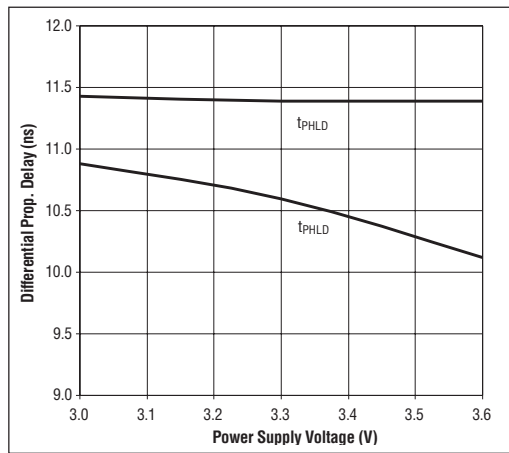


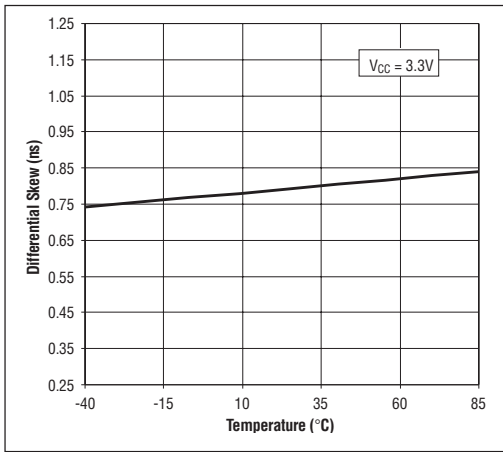*Figure 10. Differential Propagation Delay vs Voltage*



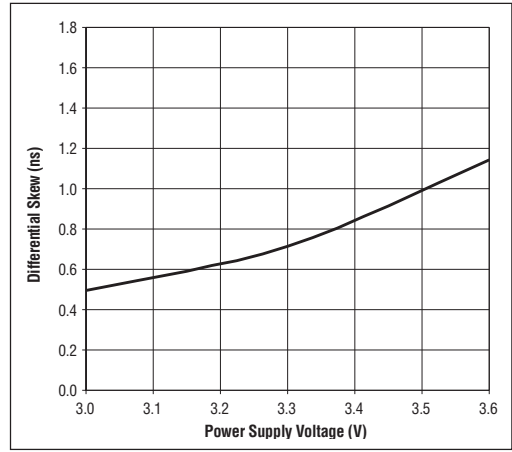*Figure 11. Differential Skew vs Temperature*



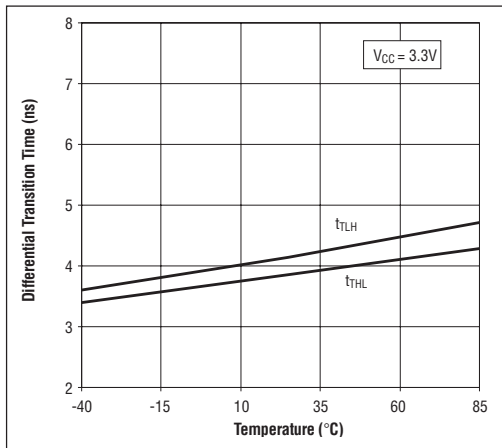*Figure 12. Differential Skew vs Voltage*



*Figure 13. Differential Transition Time vs Temperature*
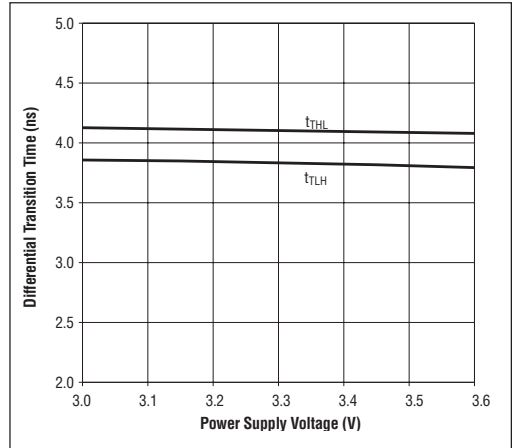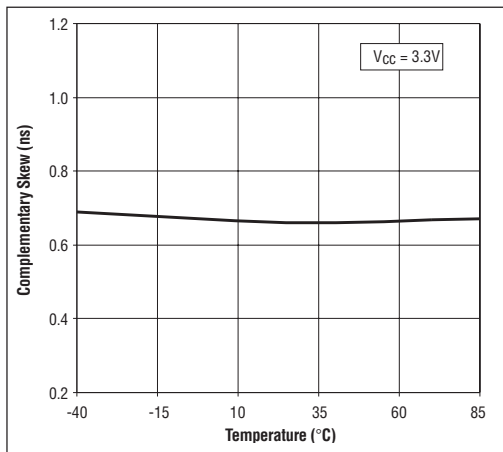


*Figure 14. Differential Transition Time vs Voltage*

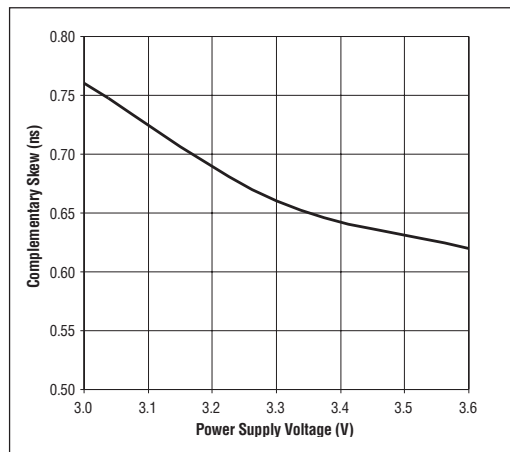*Figure 15. Complementary Skew vs Temperature*
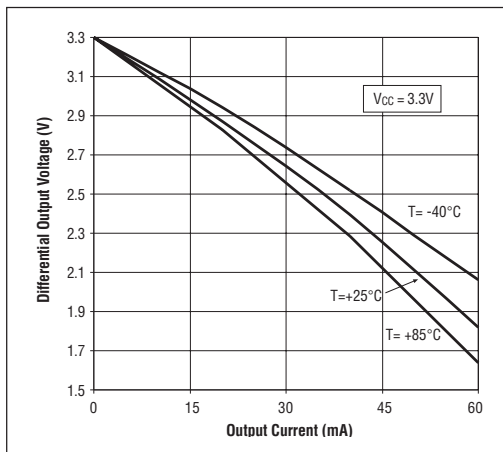


*Figure 16. Complementary Skew vs Voltage*



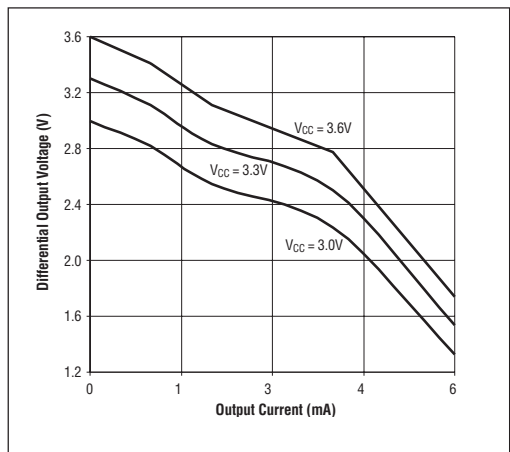*Figure 17. Differential $V_{OUT}$ vs $I_{OUT}$ (Temperature)*



*Figure 18. Differential $V_{OUT}$ vs $I_{OUT}$ ($V_{CC}$)*
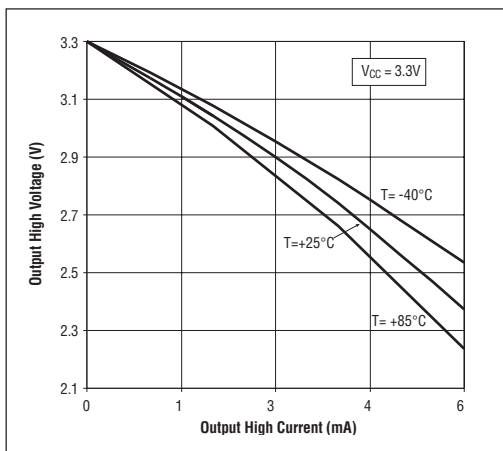


*Figure 19. $V_{OUT}$ high vs $I_{OUT}$ (Temperature)*
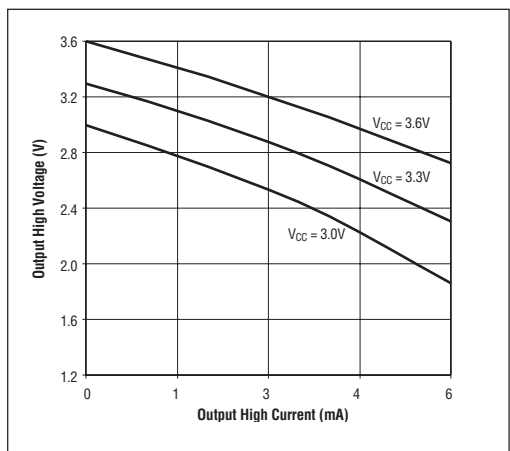


*Figure 20. $V_{OUT}$ high vs $I_{OUT}$ ($V_{CC}$)*

Date: 2/24/05          SP26LV431 High Speed, +3.3V Quad RS-422 Differential Line Driver     © Copyright 2005 Sipex Corporationn

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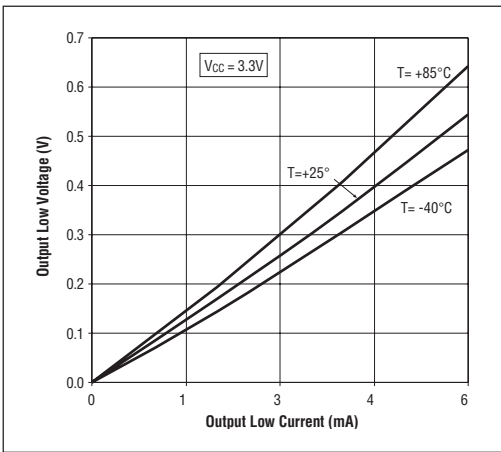
*Figure 21. V$_{OUT}$ low vs Current (Temperature)*
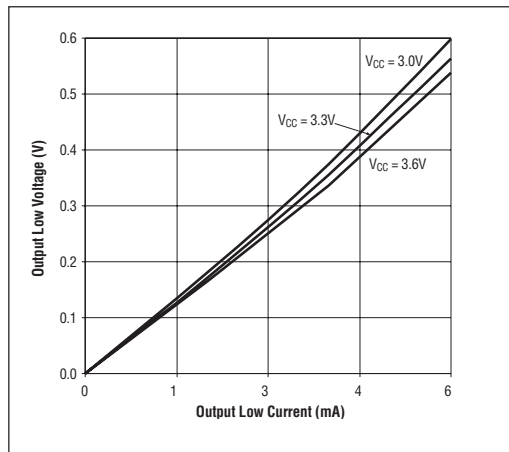


*Figure 22. V$_{OUT}$ low vs Current (V$_{CC}$)*
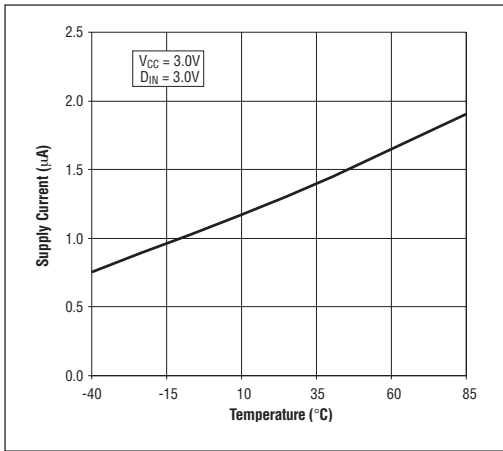


*Figure 23. Supply Current vs Temperature*
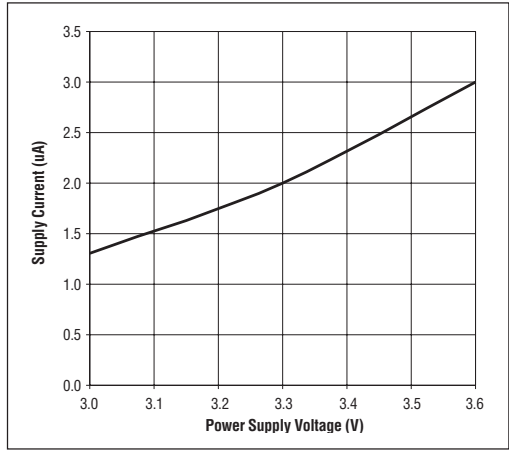


*Figure 24. Supply Current vs Voltage*
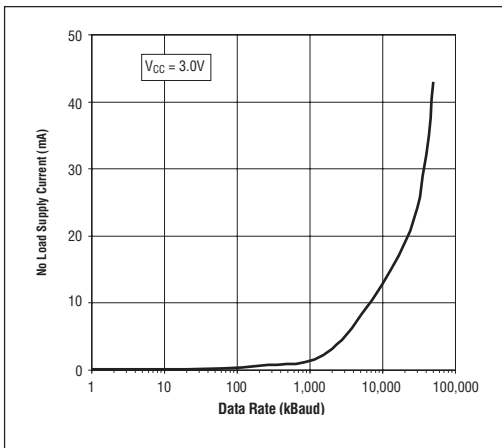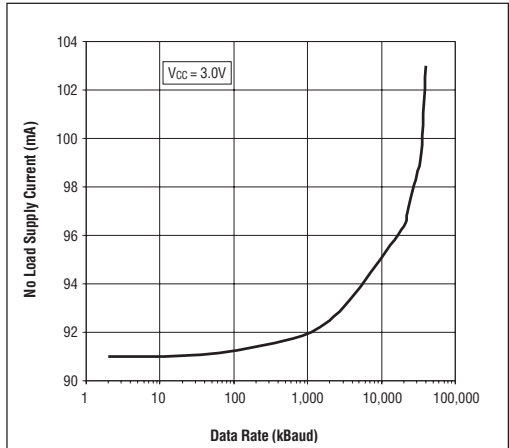


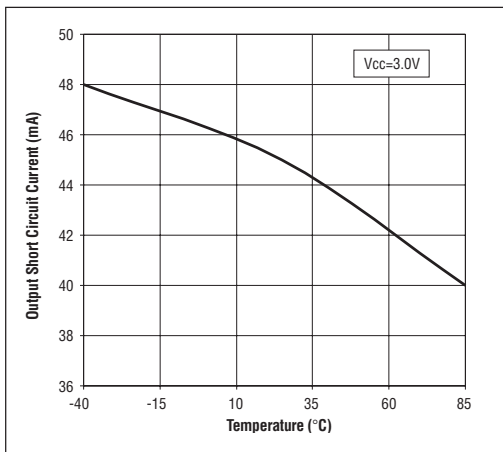*Figure 25. Supply Current vs Data Rate*



*Figure 26. I$_{CC}$ (loaded) vs Data Rate*
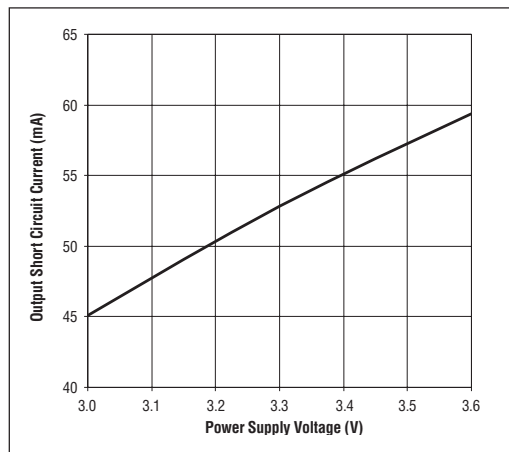
*Figure 27. Short Circuit Current vs Temperature*



*Figure 28. Short  Circuit Current vs Voltage*
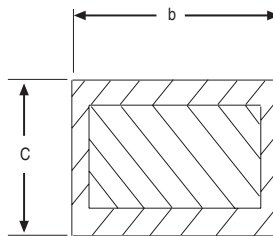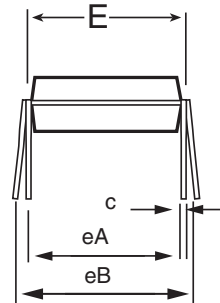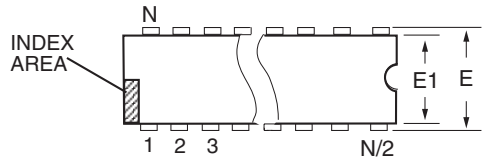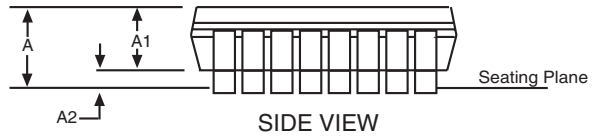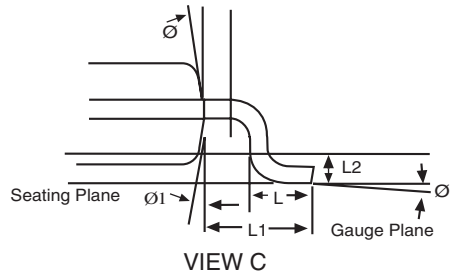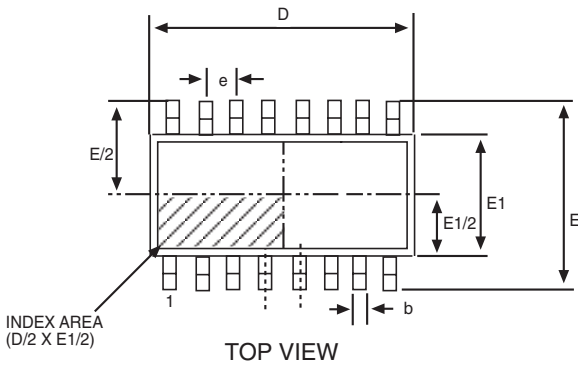
| DI$_1$ | 1 | | 16 | V$_{CC}$ |
|---|---|---|---|---|
| D0$_1$A | 2 | Sipex | 15 | DI$_4$ |
| D0$_1$B | 3 | SP26LV431 | 14 | D0$_4$A |
| ENABLE | 4 | | 13 | D0$_4$B |
| D0$_2$B | 5 | | 12 | $\overline{\text{ENABLE}}$ |
| D0$_2$A | 6 | | 11 | D0$_3$B |
| DI$_2$ | 7 | | 10 | D0$_3$A |
| GND | 8 | | 9 | DI$_3$ |
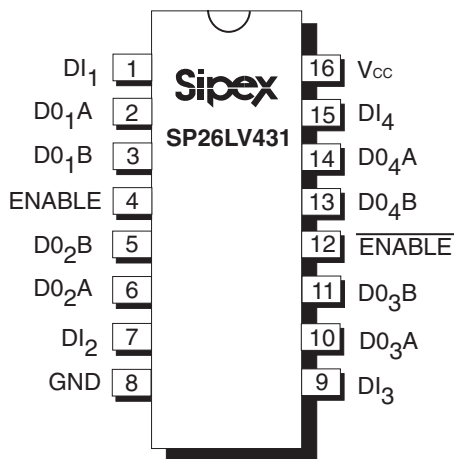
**PINOUT**

## PIN ASSIGNMENTS

| PIN NUMBER | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | DI$_1$ | Driver 1 TTL input. |
| 2 | D0$_1$A | Non-inverted driver output. |
| 3 | D0$_1$B | Inverted driver output. |
| 4 | ENABLE | Driver output enable, active HIGH. |
| 5 | D0$_2$B | Inverted driver output. |
| 6 | D0$_2$A | Non-inverted driver output. |
| 7 | DI$_2$ | Driver 2 TTL input. |
| 8 | GND | Ground. |
| 9 | DI$_3$ | Driver 3 TTL input. |
| 10 | D0$_3$A | Non-inverted driver output. |
| 11 | D0$_3$B | Inverted driver output. |
| 12 | $\overline{\text{ENABLE}}$ | Driver output enable, active LOW. |
| 13 | D0$_4$B | Inverted driver output. |
| 14 | D0$_4$A | Non-inverted driver output. |
| 15 | DI$_4$ | Driver 4 TTL input. |
| 16 | V$_{CC}$ | +3.0V to +3.6V power supply. |

| 16 PIN PDIP JEDEC MS-001 (BB) Variation | | | |
|---|---|---|---|
| SYMBOL | MIN | NOM | MAX |
| A | - | - | 0.21 |
| A1 | 0.15 | - | - |
| A2 | 0.115 | 0.13 | 0.195 |
| b | 0.014 | 0.018 | 0.022 |
| b2 | 0.045 | 0.06 | 0.07 |
| b3 | 0.3 | 0.039 | 0.045 |
| c | 0.008 | 0.01 | 0.014 |
| D | 0.735 | 0.75 | 0.755 |
| D1 | 0.005 | - | - |
| E | 0.3 | 0.31 | 0.325 |
| E1 | 0.24 | 0.25 | 0.28 |
| e | .100 BSC | | |
| eA | .300 BSC | | |
| eB | - | - | 0.43 |
| L | 0.115 | 0.13 | 0.15 |
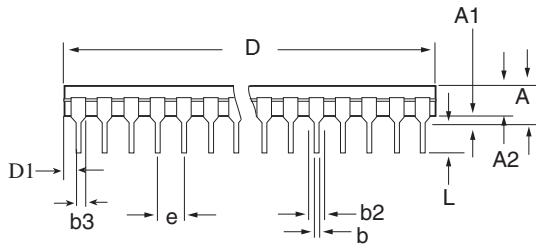
Note: Dimensions in (mm)

TOP VIEW

INDEX AREA
(D/2 X E1/2)

VIEW C

Seating Plane

Gauge Plane

SIDE VIEW

Seating Plane

| 16 Pin NSOIC JEDEC MO-012 (AC) Variation | | | |
|---|---|---|---|
| SYMBOL | MIN | NOM | MAX |
| A | 1.35 | - | 1.75 |
| A1 | 0.1 | - | 0.25 |
| A2 | 1.25 | - | 1.65 |
| b | 0.31 | - | 0.51 |
| c | 0.17 | - | 0.25 |
| D | | 9.90 BSC | |
| E | | 6.00 BSC | |
| E1 | | 3.90 BSC | |
| e | | 1.27 BSC | |
| L | 0.4 | - | 1.27 |
| L1 | | 1.04 REF | |
| L2 | | 0.25 BSC | |
| ø | 0º | - | 8º |
| ø1 | 5º | - | 15º |
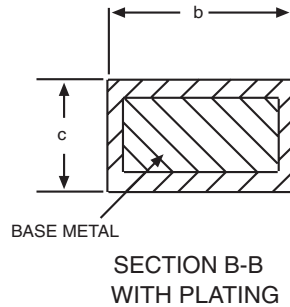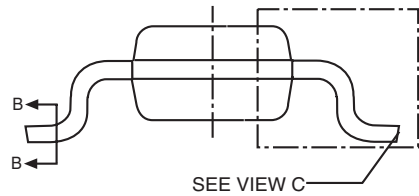
Note: Dimensions in (mm)

SEE VIEW C

BASE METAL

SECTION B-B
WITH PLATING

## ORDERING INFORMATION

*CLICK HERE TO ORDER SAMPLES*

## REVISION HISTORY

| DATE | REVISION | DESCRIPTION |
|---|---|---|
| 3/08/04 | A | Production Release. |
| 2/24/05 | B | Include tape and reel p/n's. |
| | | |

# Sipex
Corporation

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