Stellaris® LM3S5B91 RevC5 Errata

This document contains known errata at the time of publication for the Stellaris LM3S5B91 microcontroller. The table below summarizes the errata and lists the affected revisions. See the data sheet for more details.

See also the ARM® Cortex™-M3 errata, ARM publication number PR326-PRDC-009450 v2.0.

Table 1. Revision History

Date	Revision	Description
October 2012	2.3	■ Clarified issue “Debug interface is reset by any type of reset” on page 6. ■ Added issue “JTAG state machine may advance after certain resets” on page 9. ■ Added issue “Non-word-aligned write to SRAM can cause incorrect value to be loaded” on page 11. ■ Added issue “Internal reset supervisors may not prevent incorrect device operation during power transitions” on page 12. ■ Added issue “Watchdog clear mechanism described in the data sheet does not work for the Watchdog Timer 1 module” on page 25. ■ Added issue “Watchdog Timer 1 module asserts reset signal even if not programmed to reset” on page 25. ■ Added issue “WDTLOAD yields an incorrect value when read back” on page 26. ■ Added issue “Digital comparator in last step of sequence does not trigger or interrupt” on page 28. ■ Added issue “Digital comparator interrupts do not trigger or interrupt as expected” on page 28. ■ Added issue “Missing trigger or interrupt when multiple sequences configured for processor trigger and different trigger” on page 28. ■ Added issue “ADC sample sequencers priorities are different than expected” on page 29. ■ Added issue “When UART LIN or SIR mode is enabled, µDMA burst transfer does not occur” on page 30. ■ Added issue “UART transfers fail at certain system clock frequency and baud rate combinations” on page 31. ■ Added issue “Freescale SPI Mode at low SSIClk frequencies can yield data corruption” on page 31. ■ Added issue “First two ADC samples from the internal temperature sensor must be ignored” on page 36.
June 2012	2.2	■ Clarified how to read the date code on Stellaris devices. ■ Clarified wording of issue “USB0DM may be driven after reset” on page 35.

Date	Revision	Description
March 2011	2.1	■ Removed issue "The Reset Cause register always reports POR regardless of reset type" as it does not affect this device. ■ Added issue “In Host-Bus 16 mode, only one byte select is asserted if only 8 bits are read” on page 19. ■ Added issue “When non-blocking reads are pending, EPI accesses can cause the NBRFIFO counter to be incorrectly decremented” on page 19. ■ Added issue “In General-Purpose mode, the framing signal is output regardless of the state of the FRMPIN bit” on page 19. ■ Added issue “In General-Purpose mode, the maximum time to wait for the iRDY signal is derived from the system clock, not the EPI clock” on page 20. ■ Added issue “USB0DM may be driven after reset” on page 35.
September 2011	2.0	■ Started tracking revision history. ■ Added issue “Boundary scan is not functional” on page 4. ■ Added issue "The Reset Cause register always reports POR regardless of reset type". ■ Added issue “At EPI clock speeds over 15 MHz, SDRAM initialization delay is not long enough” on page 18. ■ Added issue “LIN mode Sync Break does not have the correct length” on page 30.

Table 2. List of Errata

Erratum Number	Erratum Title	Module Affected	Revision(s) Affected
1.1	Boundary scan is not functional	JTAG	C5
2.1	The PIOSC cannot be calibrated by the user	System Control	C5
2.2	The MINOR field in Device Identification 0 (DID0) register is incorrect	System Control	C5
2.3	Debug interface is reset by any type of reset	System Control	C5
2.4	JTAG state machine may advance after certain resets	System Control	C5
2.5	Non-word-aligned write to SRAM can cause incorrect value to be loaded	System Control	C5
2.6	Internal reset supervisors may not prevent incorrect device operation during power transitions	System Control	C5
3.1	Deep-Sleep mode must not be used	Flash Memory	C5
3.2	Mass erase must not be used if Flash protection bits are used	Flash Memory	C5
3.3	Page erase or program must not be performed on a protected Flash page	Flash Memory	C5
3.4	Flash memory endurance cycle specification is 100 cycles	Flash Memory	C5
4.1	The µDMA controller fails to generate capture mode DMA requests from Timer A in the Timer modules	µDMA	C5
4.2	The µDMA does not generate a completion interrupt when transferring to and from GPTM 2A and 2B	µDMA	C5

Erratum Number	Erratum Title	Module Affected	Revision(s) Affected
5.1	PB1 has permanent internal pull-up resistance	GPIO	C5
6.1	At EPI clock speeds over 15 MHz, SDRAM initialization delay is not long enough	EPI	C5
6.2	In Host-Bus 16 mode, only one byte select is asserted if only 8 bits are read	EPI	C5
6.3	When non-blocking reads are pending, EPI accesses can cause the NBRFIFO counter to be incorrectly decremented	EPI	C5
6.4	In General-Purpose mode, the framing signal is output regardless of the state of the FRMPIN bit	EPI	C5
6.5	In General-Purpose mode, the read and write strobes are output regardless of the state of the RW bit	EPI	C5
6.6	In General-Purpose mode, the maximum time to wait for the iRDY signal is derived from the system clock, not the EPI clock	EPI	C5
7.1	The General-Purpose Timer match register does not function correctly in 32-bit mode	General-Purpose Timers	C5
7.2	A spurious DMA request is generated when the timer rolls over in Input-Edge Time mode	General-Purpose Timers	C5
7.3	A spurious DMA request is generated when the timer rolls over the 16-bit boundary	General-Purpose Timers	C5
7.4	The value of the prescaler register is not readable in Edge-Count mode	General-Purpose Timers	C5
7.5	ADC trigger and Wait-on-Trigger may assert when the timer is disabled	General-Purpose Timers	C5
7.6	Wait-on-Trigger does not assert unless the TnOTE bit is set	General-Purpose Timers	C5
7.7	Do not enable match and timeout interrupts in 16-bit PWM mode	General-Purpose Timers	C5
7.8	Do not use µDMA with 16-bit PWM mode	General-Purpose Timers	C5
7.9	Writing the GPTMTnV register does not change the timer value when counting up	General-Purpose Timers	C5
7.10	The prescaler does not work correctly when counting up in periodic or one-shot mode	General-Purpose Timers	C5
7.11	Snapshot must be enabled in both Timer A and B when in 32-bit snapshot mode	General-Purpose Timers	C5
8.1	Writes to Watchdog Timer 1 module WDTLOAD register sometimes fail	Watchdog Timers	C5
8.2	Watchdog clear mechanism described in the data sheet does not work for the Watchdog Timer 1 module	Watchdog Timers	C5
8.3	Watchdog Timer 1 module asserts reset signal even if not programmed to reset	Watchdog Timers	C5
8.4	WDTLOAD yields an incorrect value when read back	Watchdog Timers	C5
9.1	ADC hardware averaging produces erroneous results in differential mode	ADC	C5

Erratum Number	Erratum Title	Module Affected	Revision(s) Affected
9.2	Differential pair encodings are incorrect	ADC	C5
9.3	Retriggering a sample sequencer before it has completed the current sequence results in continuous sampling	ADC	C5
9.4	Digital comparator in last step of sequence does not trigger or interrupt	ADC	C5
9.5	Digital comparator interrupts do not trigger or interrupt as expected	ADC	C5
9.6	Missing trigger or interrupt when multiple sequences configured for processor trigger and different trigger	ADC	C5
9.7	ADC sample sequencers priorities are different than expected	ADC	C5
10.1	The RTRIS bit in the UARTRIS register is only set when the interrupt is enabled	UART	C5
10.2	LIN mode Sync Break does not have the correct length	UART	C5
10.3	When UART LIN or SIR mode is enabled, µDMA burst transfer does not occur	UART	C5
10.4	UART transfers fail at certain system clock frequency and baud rate combinations	UART	C5
11.1	Freescale SPI Mode at low SSIClk frequencies can yield data corruption	SSI	C5
12.1	USB paired JK jitter compliance test requires automatic waiver	USB	C5
12.2	USB low speed crossover voltage compliance test requires automatic waiver	USB	C5
12.3	MCU may fail USB certification if the EPI module is operating	USB	C5
12.4	Special considerations for PB1	USB	C5
12.5	Cannot communicate with a low-speed Device through a hub	USB	C5
12.6	USB0DM may be driven after reset	USB	C5
13.1	PWM fault latch does not operate correctly	PWM	C5
14.1	First two ADC samples from the internal temperature sensor must be ignored	Electrical Characteristics	C5

1 JTAG

1.1 Boundary scan is not functional

Description:

The boundary scan is not functional on this device.

Workaround:

None.

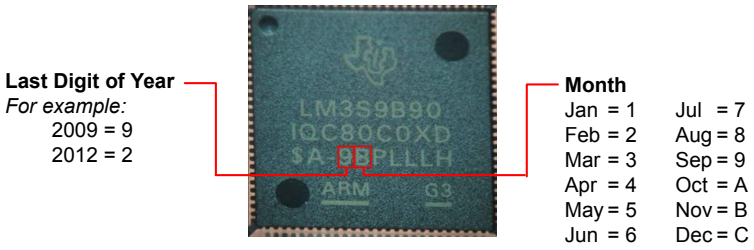
Silicon Revision Affected:

C5

Fixed:

Fixed on devices with date codes of 1A (October, 2011) or later.

Note: To determine the date code of your part, look at the first two characters following the dash on the third line of the part markings (highlighted in red in the following figure). The first number after the dash indicates the last decimal digit of the year. The second character indicates the month. Therefore, the following example shows a date code of 9B which indicates November 2009.



2 System Control

2.1 The PIOSC cannot be calibrated by the user

Description:

The PIOSC is trimmed by the factory, but cannot be user calibrated using the UPDATE bit in the **Precision Internal Oscillator Calibration (PIOSCCAL)** register.

Workaround:

None.

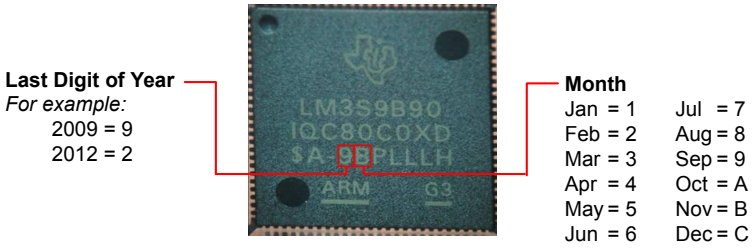
Silicon Revision Affected:

C5

Fixed:

Fixed on devices with date codes of 17 (July, 2011) or later.

Note: To determine the date code of your part, look at the first two characters following the dash on the third line of the part markings (highlighted in red in the following figure). The first number after the dash indicates the last decimal digit of the year. The second character indicates the month. Therefore, the following example shows a date code of 9B which indicates November 2009.



2.2 The MINOR field in Device Identification 0 (DID0) register is incorrect

Description:

The MINOR field, bits[7:0], in the **Device Identification 0 (DID0)** register is incorrect. The MINOR field should be 0x05 indicating the fifth metal layer change. Instead, the field reads as 0x04.

Workaround:

None.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

2.3 Debug interface is reset by any type of reset

Description:

The Serial Wire JTAG Debug Port (SWJ-DP) is reset by any reset condition. Therefore, any access to a debugger is lost, including breakpoints, watchpoints, vector catch, and trace. These reset types include:

- Watchdog reset
- Brown-out reset
- Software reset
- Reset pin assertion
- Main oscillator fail

Normal operation of the device is not affected by the reset of the SWJ-DP, however, users should bear this functionality in mind during development and debugging of applications. If a debugger does a SYSRESREQ, or if the debugger is being used in a session and a system reset occurs due to one of the reset sources above, then the debugger loses its state, including breakpoints, watchpoints, vector catch, and trace. Most debuggers attempt a recovery, usually after reporting the error to the user. If the debugger is able to recover control, the state of the application at that time reflects that the code has been running from reset and has not stopped on any breakpoints. If the application has breakpoint instructions physically in the code, such as for system calls that run through the debugger, then the code will have entered the fault handlers.

Another consequence of this erratum is that the USB may fail to enumerate when using a debugger. When debugging a board with USB and a crystal with a frequency greater than 8 MHz, the debugger writes the **RCC** register with the XTAL value for 8 MHz. As a result, the USB PLL cannot lock onto the required frequency and requires a hard reset.

Workaround:

Because some ARM debuggers expect to maintain connectivity when a system reset is requested, the SYSRESREQ bit in the **Application Interrupt and Reset Control (APINT)** register should not be used when using these debuggers; instead the VECTRESET bit, which only resets the core,

should be used so that debug connectivity is uninterrupted. VECTRESET does not reset on-chip peripherals, which must be reset with specific reset operations.

When debugging code that requires a software reset, the SYSRESREQ software reset mechanism in the NVIC (which is used by the Stellaris Peripheral Driver Library SysctlReset() and ROM_SysCtlReset() APIs) should not be used; instead, use the sequence of register writes with a VECTRESET in the NVIC as shown in the code below.

In addition, the ROM is mapped into address 0x0 during reset. The ROM code determines if boot loading is needed, and if not, transfers control to the normal application in Flash memory. As a result, the ROM is visible to the debugger on the reset entry. Debugging can be affected during Flash memory verification because the debugger compares the expected image with the ROM contents and not the Flash memory as intended. The disassembly shown to the user is also affected. To avoid these issues, debuggers must switch off the ROM mapping. However, if the debugger in use does not switch off the ROM, the user can either step through the first assembly instructions until the ROM gets remapped or write a 1 to the BA bit in the **ROM Control (ROMCTL)** register at location 0x400F.E0F0 using the debugger GUI, debugger command line, or debugger startup script.

Use of any reset source listed above other than software reset causes the debugger to lose connectivity.

A consequence to using VECTRESET and a debugger simultaneously, as described in the workaround, is that the USB may fail to enumerate when using a debugger. When debugging a board with USB and a crystal with a frequency greater than 8 MHz, the debugger writes the **RCC** register with the XTAL value for 8 MHz. As a result, the USB PLL cannot lock onto the required frequency and requires a hard reset.

When debugging with USB and a crystal greater than 8 MHz, always disable the USB PLL before writing the **RCC** XTAL value to ensure that the USB PLL starts up correctly.

```
//
// Disable processor interrupts.
//
IntMasterDisable();

//
// Disable the PLL and the system clock divider (this is a NOP if they are
// already disabled).
//
HWREG(SYSCTL_RCC) = ((HWREG(SYSCTL_RCC) & ~(SYSCTL_RCC_USESYSDIV)) |
                     SYSCTL_RCC_BYPASS);
HWREG(SYSCTL_RCC2) |= SYSCTL_RCC2_BYPASS2;

//
// Now, write RCC and RCC2 to their reset values.
//
HWREG(SYSCTL_RCC) = 0x078e3ad0 | (HWREG(SYSCTL_RCC) & SYSCTL_RCC_MOSCDIS);
HWREG(SYSCTL_RCC2) = 0x07806810;
HWREG(SYSCTL_RCC) = 0x078e3ad1;

//
// Reset the deep sleep clock configuration register.
//
HWREG(SYSCTL_DSLPCLKCFG) = 0x07800000;

//
// Reset the clock gating registers.
```

```
//
HWREG(SYSCTL_RCGC0) = 0x00000040;
HWREG(SYSCTL_RCGC1) = 0;
HWREG(SYSCTL_RCGC2) = 0;
HWREG(SYSCTL_SCGC0) = 0x00000040;
HWREG(SYSCTL_SCGC1) = 0;
HWREG(SYSCTL_SCGC2) = 0;
HWREG(SYSCTL_DCGC0) = 0x00000040;
HWREG(SYSCTL_DCGC1) = 0;
HWREG(SYSCTL_DCGC2) = 0;

//
// Reset the remaining SysCtl registers.
//
HWREG(SYSCTL_PBORCTL) = 0;
HWREG(SYSCTL_IMC) = 0;
HWREG(SYSCTL_GPIOHBCTL) = 0;
HWREG(SYSCTL_MOSCCTL) = 0;
HWREG(SYSCTL_PIOSCCAL) = 0;
HWREG(SYSCTL_I2SMCLKCFG) = 0;

//
// Reset the peripherals.
//
HWREG(SYSCTL_SRCR0) = 0xffffffff;
HWREG(SYSCTL_SRCR1) = 0xffffffff;
HWREG(SYSCTL_SRCR2) = 0xffffffff;
HWREG(SYSCTL_SRCR0) = 0;
HWREG(SYSCTL_SRCR1) = 0;
HWREG(SYSCTL_SRCR2) = 0;

//
// Clear any pending SysCtl interrupts.
//
HWREG(SYSCTL_MISC) = 0xffffffff;

//
// Wait for any pending flash operations to complete.
//
while((HWREG(FLASH_FMC) & 0xffff) != 0)
{
}
while((HWREG(FLASH_FMC2) & 0xffff) != 0)
{
}

//
// Reset the flash controller registers.
//
HWREG(FLASH_FMA) = 0;
HWREG(FLASH_FCIM) = 0;
HWREG(FLASH_FCMISC) = 0xffffffff;
HWREG(FLASH_FWBVAL) = 0;
```

```
//
// Issue the core reset.
//
HWREG(NVIC_APINT) = NVIC_APINT_VECTKEY | NVIC_APINT_VECT_RESET;
```

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

2.4 JTAG state machine may advance after certain resets

Description:

Due to an issue with the reset logic, the JTAG state machine may advance to a random state if one of the following resets occurs:

- Hardware Reset via the $\overline{\text{RST}}$ pin
- Brown-Out Reset
- Software System Request Reset (using SYSRESREQ)
- Watchdog Reset
- MOSC Failure Reset

On most devices, these state transitions do not cause any noticeable problems. Some devices, however, eventually execute random JTAG instructions after multiple resets of the type listed above. Since some JTAG instructions can interfere with device operation, steps must be taken to avoid this behavior in a production environment.

In a development environment where a JTAG debugger is being used, this issue is likely to go unnoticed. Many JTAG debuggers pull TCK Low after establishing a connection with the device, which prevents the random state transitions from happening. Also, many JTAG debuggers reset the microcontroller using VECTRESET instead of SYSRESREQ, which also avoids the problem.

Workaround:

There are two workarounds, each with trade-offs:

- Connect TCK to GND through a 10-K resistor in the final board design. This avoids the problem completely but it causes the chip to draw a small amount of additional current, since the default pin configuration of TCK includes a weak internal pull-up resistor.
- Implement a software routine to explicitly reset the JTAG state machine after every system reset. This works for most cases, but it does not protect the ROM boot loader from erroneous JTAG instruction execution.

```
void
ResetJTAGState(void)
{
    volatile unsigned char ucToggleCount, ucDelayCount;

    //
```

```
    // Enable GPIO port C
    //
    HWREG(SYSCTL_RCGC2) = SYSCTL_RCGC2_GPIOC;

    //
    // Dummy read to make sure GPIO port C has time to enable before we
    // proceed.
    //
    ucToggleCount = HWREG(SYSCTL_RCGC2);

    //
    // Unlock the GPIOs on port C
    //
    HWREG(GPIO_PORTC_BASE + GPIO_O_LOCK) = GPIO_LOCK_KEY_DD;
    HWREG(GPIO_PORTC_BASE + GPIO_O_CR) = 0x01;

    //
    // "Toggle" TCK at least 5 times while TMS remains high. We're relying on a
    // digitally disabled pin to feed a "zero" into the JTAG module, and we're
    // also relying on an external pull-up to feed us our "one". To be extra
    // conservative, let's try 10 toggles.
    //
    for(ucToggleCount = 0; ucToggleCount < 10; ucToggleCount++)
    {
        //
        // Turn off the digital enable for PC0
        //
        HWREG(GPIO_PORTC_BASE + GPIO_O_DEN) &= ~(0x01);

        //
        // Delay a little to make sure the signal propagates through the JTAG
        // state machine (make sure these delays do not get optimized out by
        // the compiler).
        //
        for(ucDelayCount=0; ucDelayCount<100; ucDelayCount++)
        {
        }

        //
        // Turn on the digital enable for PC0
        //
        HWREG(GPIO_PORTC_BASE + GPIO_O_DEN) |= 0x01;

        //
        // Delay a little
        //
        for(ucDelayCount=0; ucDelayCount<100; ucDelayCount++)
        {
        }
    }
}
```

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

2.5 Non-word-aligned write to SRAM can cause incorrect value to be loaded

Description:

If a word-aligned value is loaded from an SRAM location into a core register, then altered by storing a byte or halfword at an unaligned offset, the altered word-aligned value is not correctly indicated when loaded into a core register. The loaded value from the SRAM location into a core register reflects the original value, not the modified value.

The following assembly sequence causes the altered value loaded into a core register to not load the correct value, even though the correct value is visible in the SRAM memory location.

```
//
// Load a word-aligned value from an SRAM location into a
// core register (such as R0)
//
LDR        R0, [SP, #+0];

//
// Store byte or halfword from the core register to
// the SRAM location at a non-word-aligned offset
//
STRB     R0, [SP, #+1];
      OR
STRB     R0, [SP, #+2];
      OR
STRB     R0, [SP, #+3];
      OR
STRH     R0, [SP, #+1];

//
// Load the same word-aligned value of the same SRAM location
// into a core register (such as R0)
//
LDR       R0, [SP, #+0];
```

This assembly sequence causes erroneous values only if these three instructions are executed in this order. However, the three instructions do not have to be consecutive, which means that other instructions can be placed in between the first and the second instructions, or the second and the third instructions, and the false value still occurs. Other instructions include, but are not limited to, branches in Flash, accesses to non-SRAM locations such as peripherals, and writes to other SRAM locations.

Pointers, structures, and unions are common C code methods that can be found in user code that may generate this assembly sequence and, therefore, result in incorrect values for variables. If using interrupts, it is possible to continue the assembly sequence in the interrupt handler, which could also return incorrect data.

For more information about this erratum as well as C code examples that may generate this assembly sequence, refer to the document, *Non-Word-Aligned Write to SRAM Additional Information* (SPMA047).

Workaround:

The type of compiler and optimization settings used in your application affects whether the problematic assembly code is generated from your user code. Each compiler behaves a little differently with respect to this erratum. The behavior for each compiler is not guaranteed due to the large number of compiler and tool version combinations.

At the assembly level, loading a volatile 32-bit-aligned word value from a different address in SRAM after storing and before loading in the assembly instruction sequence yields a correct value. A dummy SRAM load of a volatile 32-bit-aligned word from a different SRAM memory location should be inserted after the second assembly instruction (storing a byte or halfword from the core register to the desired SRAM location at a non-word-aligned offset) and before the third assembly instruction (loading the same word-aligned value of the desired SRAM location into a core register). This also means that a dummy SRAM load of a volatile 32-bit-aligned word from a different SRAM memory location should also be placed at the beginning of any interrupt routine, in case the third assembly instruction is executed before leaving the handler.

For more information about this erratum as well as C code examples that may generate this assembly sequence, refer to the document, *Non-Word-Aligned Write to SRAM Additional Information* (SPMA047).

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

2.6 Internal reset supervisors may not prevent incorrect device operation during power transitions

Description:

This microcontroller incorporates internal Power-On Reset (POR) and Brown-Out Reset (BOR) supervisors to ensure that code only executes when power to the device is within specification. However, gaps in the voltage and timing thresholds of the internal supervisors result in a risk of incorrect operation during VDD power transitions.

Unexpected operation may occur that can include brief execution of random sections of user code including ROM functions and random instructions, as well as incorrect power-up initialization. The uncontrolled brief execution of random instructions may result in the undesired erasing or writing of non-volatile memories and GPIO state changes. There is also the possibility that the device may be left in a state where it does not operate correctly until a clean power cycle has been completed.

The Power-On Reset gap occurs because the supervisor can release internal state machine operation as soon as 6.0 ms after the VDD supply reaches 1.9 V. If VDD is still below the minimum operating voltage of 3.0 V after 6.0 ms, the power-up state machine may not function correctly, resulting in the effects described above. The $\overline{\text{RST}}$ pin of the device has no effect on the initialization state machine, therefore, a complete power-cycle is required to restore the initialization state machine.

The Brown-Out Reset threshold (V_{BTH}) gap occurs because the brown-out supervisor has a threshold as low as 2.85 V, which is less than the minimum operating voltage on VDD, and also because it can take several microseconds to respond. BOR gaps can be encountered after power up, during steady state operation power-on, if the VDD rail has glitches, and also during power-down.

Workaround:

After initial power-up, any processor operation with VDD below 3.0 V may result in unexpected code execution resulting in the effects described above. The processor must be halted or the $\overline{\text{RST}}$ signal must be driven Low prior to VDD dropping below 3.0 V and stay in that state until VDD is above 3.0 V.

If VDD falls below 2.1 V, it must continue to fall until it reaches 1.5 V. VDD must stay below 1.5 V for at least 36 µs to ensure that a POR is triggered correctly. Additionally, the VDD power-up time between 1.9 V and 3.0 V must be at most 6.0 ms. If VDD falls below 3.0 V but stays above 2.1 V, it is not necessary for the voltage to continue falling below 2.1 V. VDD can come back up to 3.0 V without any additional timing requirements.

The system designer must ensure they meet the requirements listed below for power-up, steady state, and power-down:

1. The VDD power-up, steady state, and power-down waveform meets the timing requirements shown in Figure 1 on page 14.
2. The power-up transition of VDD between 1.9 V and 3.0 V must not have any points where it decreases in voltage (must be monotonic).
3. The power-down transition of VDD between 3.0 V and 1.5 V must not have any points where it increases in voltage (must be monotonic).
4. Once steady-state operation between 3.0 V and 3.6 V is achieved, $\overline{\text{RST}}$ must go Low or the CPU execution must be halted prior to VDD falling below 3.0 V.
5. The **Brown-Out Reset Control (PBORCTL)** register must be set so that a brown-out event causes a reset.

Depending on the system environment requirement, items 3, 4, and 5 in the above list may be met by using a voltage supervisor, such as the TLV803M, to monitor a higher voltage rail from which the VDD supply is regulated. Figure 2 on page 14 shows this implementation with a voltage supervisor monitoring the 5-V rail and a voltage trip point of 4.38 V. A voltage supervisor with a lower voltage trip point can be used to monitor the VDD (3.3-V) rail, however this supervisor must assert reset before VDD reaches 3.0 V. Regardless of the implemented voltage supervisor circuit, the system designer must ensure that there is enough time to assert $\overline{\text{RST}}$ Low prior to VDD falling below 3.0 V. Figure 3 on page 15 shows the resulting waveform of the circuit shown in Figure 2 on page 14.

Figure 1. VDD Waveform Signature Limits

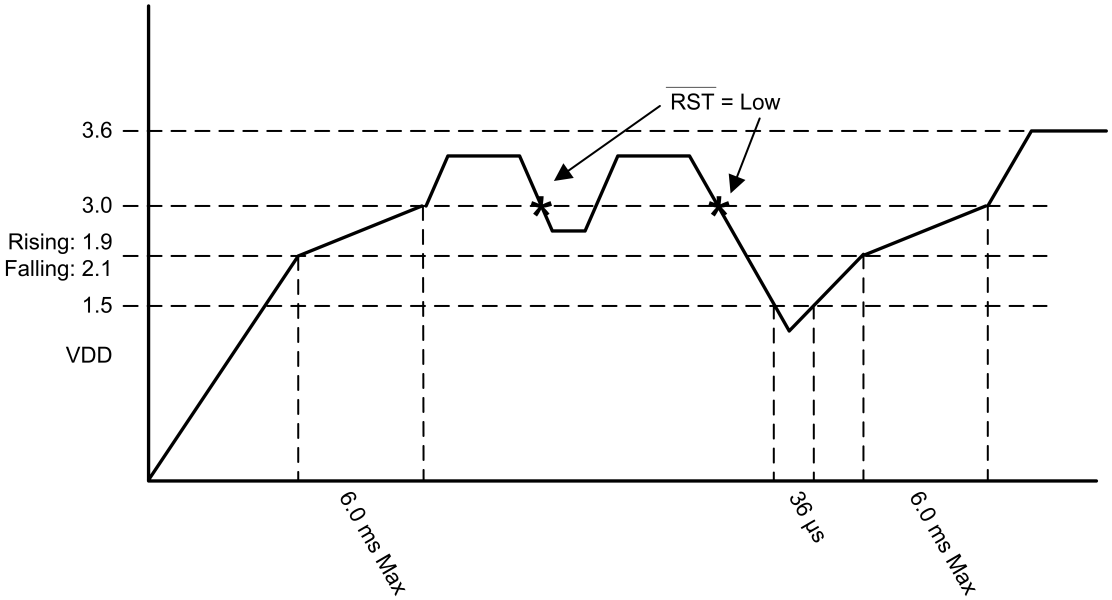


Figure 2. Using a Voltage Supervisor to Monitor the Voltage Rail

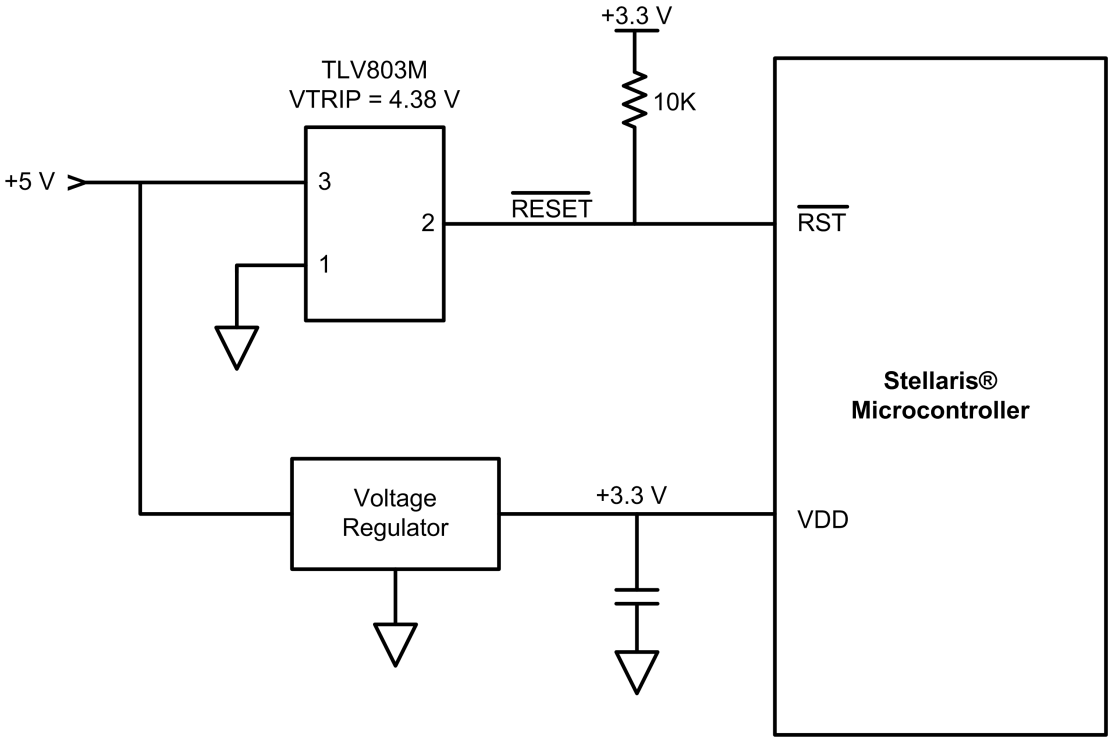
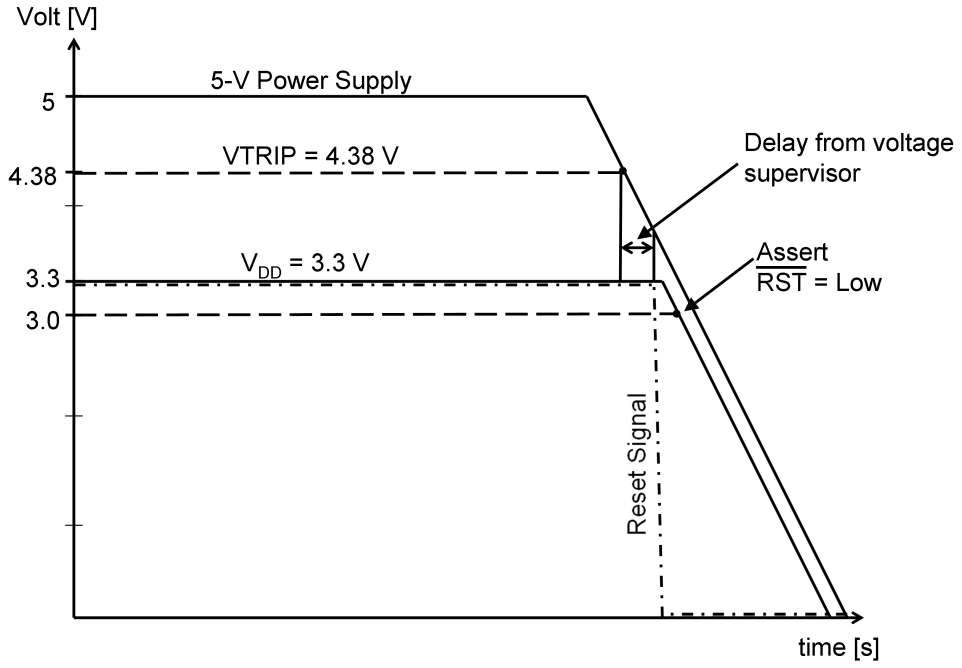


Figure 3. Resulting Waveform Using the Voltage Supervisor Circuit



Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

3 Flash Memory

3.1 Deep-Sleep mode must not be used

Description:

Deep-sleep mode must not be used.

Due to this erratum, the use of this device in USB bus-powered applications is prohibited because sleep mode current consumption exceeds the USB specification.

Workaround:

Use Sleep or Hibernation mode.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

3.2 Mass erase must not be used if Flash protection bits are used

Description:

The mass erase function using the MERASE bit in the **Flash Memory Control (FMC)** register must not be used in systems that clear any of the **Flash Memory Protection Program Enable n (FMPPEn)** bits. For Rev C3 and C5 devices, mass erase can be used as long as none of the **FMPPEn** bits are cleared.

Workaround:

Erase Flash memory with the page erase function using the ERASE bit in the **FMC** register instead of the mass erase function.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

3.3 Page erase or program must not be performed on a protected Flash page

Description:

The erase function using the ERASE bit in the **Flash Memory Control (FMC)** register and the program function using the WRITE bit in the **FMC** register or the WRBUF bit in the **FMC2** register must not be used in systems that clear the bit in **FMPPEn** that corresponds to that page of Flash. For Rev C3 and C5 devices, erase and program can be used as long as neither of the corresponding **FMPPEn** bits are cleared.

Workaround:

Only erase and program memory that is not protected by the corresponding **FMPPEn** bits.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

3.4 Flash memory endurance cycle specification is 100 cycles

Description:

The Flash memory endurance cycle specification (maximum program/erase cycles) is 100 cycles. Failure to adhere to the maximum number of program/erase cycles could result in corruption of the Flash memory contents and/or permanent damage to the device.

Workaround:

None. Because the failure mechanism is a function of the third-party Flash memory technology used in this device, there is no workaround. This third-party Flash memory technology is used only in the affected 130-nm Stellaris products and will not be used in any future devices. All other Stellaris products use Flash memory technology that exceeds industry quality and endurance cycle standards.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

4 µDMA

4.1 The µDMA controller fails to generate capture mode DMA requests from Timer A in the Timer modules

Description:

The µDMA controller fails to generate DMA requests from Timer A in the General-Purpose Timer modules when in the Event Count and Event Time modes.

Workaround:

Use Timer B.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

4.2 The µDMA does not generate a completion interrupt when transferring to and from GPTM 2A and 2B

Description:

The µDMA module does not generate a completion interrupt on the Timer 2 interrupt vector when transferring data to and from Timers 2A and 2B. The µDMA can successfully transfer data to and from Timers 2A and 2B; however, there is no interrupt to indicate that the transfer is complete.

Workaround:

If a completion interrupt is required, use an alternate GPTM.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

5 GPIO

5.1 PB1 has permanent internal pull-up resistance

Description:

Regardless of its configuration, PB1 has a maximum internal pull-up resistance of 800 ohms that turns on when the voltage on the pin is approximately 1.2 V. Due to this internal resistance, up to 3 mA of current may be sourced during the transition from 1.2 V to 3.3 V.

Workaround:

When this pin is configured as an input, the external circuit must drive with an impedance less than or equal to 300 Ω to provide enough drive strength to over-drive the internal pull-up and achieve the necessary V_{IL} voltage level. Ensure that the driver can sink the temporary current. In addition, do not use PB1 in open-drain mode.

if this pin is configured as an output, be aware that if the output was driven high and a non-POR reset occurs, the output may be driven high after reset unless it has a 300-Ω resistor on it. Once the pin is configured as an output, the pin drives the programmed level.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

6 EPI

6.1 At EPI clock speeds over 15 MHz, SDRAM initialization delay is not long enough

Description:

After enabling the EPI SDRAM interface via the **EPISDRAMCFG** register, the EPI SDRAM controller should hold off any SDRAM accesses for 100 µs. When an EPI clock speed greater than 15 MHz is used, it is possible for an access to start before the 100 µs has elapsed.

Workaround:

After enabling the EPI SDRAM interface in the **EPISDRAMCFG** register, wait 100 µs before performing any accesses to SDRAM.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

6.2 In Host-Bus 16 mode, only one byte select is asserted if only 8 bits are read

Description:

When reading from most 16-bit memories in Host-Bus 16 mode, both byte selects should be asserted for every access, even if only 8 bits are being read. The EPI controller only asserts the byte select for the required 8 bits, violating this specification.

Workaround:

For standard memory configurations, the memory operation proceeds normally. Although this behavior violates the memory specifications, the EPI reads the proper data from memory.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

6.3 When non-blocking reads are pending, EPI accesses can cause the NBRFIFO counter to be incorrectly decremented

Description:

When non-blocking reads are pending and the MCU performs a blocking read or a write from any EPI address with bits [11:4] equal to 0x07 or 0x08, the NBRFIFO counter is incorrectly decremented.

Workaround:

When a non-blocking read operation has been initiated, wait for the completion interrupt before performing any additional CPU or µDMA accesses to or from the EPI registers or the EPI memory space.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

6.4 In General-Purpose mode, the framing signal is output regardless of the state of the FRMPIN bit

Description:

In General-Purpose mode, the FRMPIN bit in the **EPI General-Purpose Configuration (EPIGPCFG)** register should control whether or not the framing signal, FRAME, is output on EPIS030. However, the FRAME signal is output regardless of the state of the FRMPIN bit.

Workaround:

If the FRMPIN signal is not required, configure the port pin to an alternate function or a GPIO.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

6.5 In General-Purpose mode, the read and write strobes are output regardless of the state of the RW bit

Description:

In General-Purpose mode, the RW bit in the **EPI General-Purpose Configuration (EPIGPCFG)** register should control whether or not the read and write strobes, RD and WR, are output on EPIS029 and EPIS028. However, the RD and WR signals are output regardless of the state of the RW bit.

Workaround:

If the read and write strobes are not required, configure the port pins to an alternate function or GPIOs.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

6.6 In General-Purpose mode, the maximum time to wait for the iRDY signal is derived from the system clock, not the EPI clock

Description:

In General-Purpose mode, the MAXWAIT field in the **EPI General-Purpose Configuration (EPIGPCFG)** register specifies the number of EPI clocks to wait for the iRDY signal to be deasserted. However, the hardware counts system clocks and not EPI clocks, so the wait may be shorter than expected.

Workaround:

Adjust the MAXWAIT configuration to account for the difference in frequency between the system clock and the EPI clock.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

7 General-Purpose Timers

7.1 The General-Purpose Timer match register does not function correctly in 32-bit mode

Description:

The **GPTM Timer A Match (GPTMTAMATCHR)** register triggers a match interrupt and a DMA request, if enabled, when the lower 16 bits match, regardless of the value of the upper 16 bits.

Workaround:

None.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

7.2 A spurious DMA request is generated when the timer rolls over in Input-Edge Time mode

Description:

When the timer is in Input-Edge Time mode and rolls over after the terminal count, a spurious DMA request is generated.

Workaround:

Either ignore the spurious interrupt, or capture the edge time into a buffer via DMA, then the spurious interrupt can be detected by noting that the captured value is the same as the previous capture value.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

7.3 A spurious DMA request is generated when the timer rolls over the 16-bit boundary

Description:

When the timer is in 32-bit periodic or one-shot mode and is enabled to generate periodic DMA requests, a spurious DMA request is generated when the timer rolls past 0x0000FFFF.

Workaround:

Only use DMA with a 16-bit periodic timer.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

7.4 The value of the prescaler register is not readable in Edge-Count mode

Description:

In Edge-Count mode, the prescaler is used as an 8-bit high order extension to the 16-bit counter. When reading the **GPTM Timer n (GPTMTnR)** register as a 32-bit value, the bits [23:16] always contain the initial value of the **GPTM Timer n Prescale (GPTMTnPR)** register, that is, the "load" value of the 8-bit extension.

Workaround:

None.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

7.5 ADC trigger and Wait-on-Trigger may assert when the timer is disabled

Description:

If the value in the **GPTM Timer n Match (GPTMTnMATCHR)** register is equal to the value of the timer counter and the TnOTE bit in the **GPTM Control (GPTMCTL)** register is set, enabling the ADC trigger, the trigger fires even when the timer is disabled (the TnEN bit in the **GPTMCTL** register is clear). Similarly, if the value in the **GPTMTnMATCHR** register is equal to the value of the timer counter and the TnWOT bit in the **GPTM Timer n Mode (GPTMTnMR)** register is set, enabling the Wait-on-Trigger mode, the trigger fires even when the timer is disabled.

Workaround:

Enable the timer before setting the TnOTE bit. Also, for the Wait-on-Trigger mode, ensure that the timers are configured in the order in which they will be triggered.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

7.6 Wait-on-Trigger does not assert unless the TnOTE bit is set

Description:

Wait-on-Trigger does not assert unless the TnOTE bit is set in the **GPTMCTL** register.

Workaround:

If the TnWOT bit in the **GPTM Timer n Mode (GPTMTnMR)** register is set, enabling the Wait-on-Trigger mode, the TnOTE bit must also be set in the **GPTMCTL** register in order for the Wait-on-Trigger to fire. Note that when the TnOTE bit is set, the ADC trigger is also enabled.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

7.7 Do not enable match and timeout interrupts in 16-bit PWM mode

Description:

16-bit PWM mode generates match and timeout interrupts in the same manner as periodic mode.

Workaround:

Ensure that any unwanted interrupts are masked in the **GPTMTnMR** and **GPTMIMR** registers.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

7.8 Do not use µDMA with 16-bit PWM mode

Description:

16-bit PWM mode generates match and timeout µDMA triggers in the same manner as periodic mode.

Workaround:

Do not use µDMA to transfer data when the timer is in 16-bit PWM mode.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

7.9 Writing the GPTMTnV register does not change the timer value when counting up

Description:

When counting up, writes to the **GPTM Timer n Value (GPTMTnV)** register do not change the timer value.

Workaround:

None.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

7.10 The prescaler does not work correctly when counting up in periodic or one-shot mode

Description:

When counting up, the prescaler does not work correctly in 16-bit periodic or snap-shot mode.

Workaround:

Do not use the prescaler when counting up in 16-bit periodic or snap-shot mode.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

7.11 Snapshot must be enabled in both Timer A and B when in 32-bit snapshot mode

Description:

When a periodic snapshot occurs in 32-bit periodic mode, only the lower 16-bit are stored into the **GPTM Timer A (GPTMTAR)** register.

Workaround:

If both the TASNAPS and TBSNAPS bits are set in the **GPTM Timer A Mode (GPTMTAMR)** register, the entire 32-bit snapshot value is stored in the **GPTMTAR** register.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

8 Watchdog Timers

8.1 Writes to Watchdog Timer 1 module WDTLOAD register sometimes fail

Description:

Due to the independent clock domain of the Watchdog Timer 1 module, writes to the **Watchdog Load (WDTLOAD)** register may sometimes fail, even though the WRC bit in the **WDTCTL1** register is set after the write occurs.

Workaround:

After performing a write to the **WDTLOAD** register, read the contents back and verify that they are correct. If they are incorrect, perform the write operation again.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

8.2 Watchdog clear mechanism described in the data sheet does not work for the Watchdog Timer 1 module

Description:

Periodically reloading the count value into the **Watchdog Timer Load (WDTLOAD)** register of the Watchdog Timer 1 module will not restart the count, as specified in the data sheet.

Workaround:

Disable the Watchdog Timer 1 module before reprogramming the counter. Alternatively, clear the watchdog interrupt status periodically outside of the interrupt handler by writing any value to the **Watchdog Interrupt Clear (WDTICR)** register.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

8.3 Watchdog Timer 1 module asserts reset signal even if not programmed to reset

Description:

Even if the reset signal is not enabled (the RESEN bit of the **Watchdog Control (WDTCTL)** register is clear), the Watchdog Timer 1 module will assert a reset signal to the system when the time-out value is reached for a second time.

Workaround:

Clear the Watchdog Timer 1 interrupt once the time-out value is reached for the first time by writing any value to the **Watchdog Interrupt Clear (WDTICR)** register.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

8.4 WDTLOAD yields an incorrect value when read back

Description:

If the Watchdog Timer 1 module is enabled and configured to run off the PIOSC, writes to the **Watchdog Load (WDTLOAD)** register yield an incorrect value when read back.

Workaround:

None.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

9 ADC

9.1 ADC hardware averaging produces erroneous results in differential mode

Description:

The implementation of the ADC averaging circuit does not work correctly when the ADC is sampling in differential mode and the difference between the voltages is approximately 0.0V.

Workaround:

Do not use hardware averaging in differential mode. Instead, use the FIFO to store results and average them in software.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

9.2 Differential pair encodings are incorrect

Description:

When using differential mode, the MUXn fields in the **ADCSSMUXn** registers should be configured to be "i" where the paired inputs are "2i" and "2i + 1". This encoding does not work for AIN8 - AIN15.

Workaround:

Use the encodings shown in the following table:

Adjacent Channels	i	MUXn Encoding
AIN0 and AIN1	0	0x0
AIN2 and AIN3	1	0x1
AIN4 and AIN5	2	0x2
AIN6 and AIN7	3	0x3
AIN8 and AIN9	4	0x8
AIN10 and AIN11	5	0x9
AIN12 and AIN13	6	0xA
AIN14 and AIN15	7	0xB

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

9.3 Retriggering a sample sequencer before it has completed the current sequence results in continuous sampling

Description:

Re-triggering a sample sequencer before it has completed its programmed conversion sequence causes the sample sequencer to continuously sample. If interrupts have been enabled, interrupts are generated at the appropriate place in the sample sequence. This problem only occurs when the new trigger is the same type as the current trigger.

Workaround:

Ensure that a sample sequence has completed before triggering a new sequence using the same type of trigger.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

9.4 Digital comparator in last step of sequence does not trigger or interrupt

Description:

If a digital comparator that is expected to trigger or interrupt is configured for the last step of a sample sequence with sequence trigger TRIGGER_PROCESSOR, TRIGGER_COMPn, TRIGGER_EXTERNAL, TRIGGER_TIMER, or TRIGGER_PWMn, the trigger or interrupt does not occur. These sequence trigger parameters should not be used when using a sample sequencer configured with only one step and a digital comparator that is expected to trigger or interrupt.

Note: Sample Sequencer 3 can only be configured for a total of one step.

Workaround:

If an extra sequence step is available in a sample sequencer, a dummy sequence step and a dummy digital comparator can be configured as the last step in the sample sequencer.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

9.5 Digital comparator interrupts do not trigger or interrupt as expected

Description:

The digital comparator configured for the ADC sample sequence step (n+1) is triggered if the voltage on the AINx input specified for step (n) meets the conditions that trigger the digital comparator for step (n+1). In this case, the conversion results are sent to the digital comparator specified by step (n+1).

Workaround:

Adjust user code or hardware to account for the fact that the voltage seen at the AINx input specified for sequence step (n) will be handled by sequence step (n+1)’s digital comparator using sequence step (n+1)’s configurations.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

9.6 Missing trigger or interrupt when multiple sequences configured for processor trigger and different trigger

Description:

If a sample sequence is configured to trigger or interrupt using a processor event and a different, consecutive sample sequence is configured to trigger or interrupt using any other event, the interrupt or trigger for the processor-triggered sample sequence will occasionally not occur, even if the processor-triggered sample sequence is configured with a higher priority.

Workaround:

None.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

9.7 ADC sample sequencers priorities are different than expected

Description:

If sample sequencer 2 (SS2) and sample sequencer 3 (SS3) have been triggered, and sample sequencer 0 (SS0) and sample sequencer 1 (SS1) have not been triggered or have already been triggered, the priority control logic compares the priorities of SS1 and SS2 rather than SS2 and SS3. For example, if SS1's priority is the highest (such as 0) and SS3's priority is higher than SS2's priority (such as SS3 = 1, SS2 = 2), SS2 is incorrectly selected to initiate the sampling conversion after SS1. If SS1's priority is the lowest (such as 3) and SS3's priority is lower than SS2's (such as SS3 = 2, SS2 = 1), SS3 is incorrectly selected as the next sample sequencer, then SS2, then SS1.

Workaround:

If only three of the four ADC sample sequencers are needed, SS0 and SS1 can be used with either SS2 or SS3. This ensures that the execution order is as expected. If all four ADC sample sequencers are needed, the highest priority conversions should be programmed into SS0 and SS1. The sequences programmed into SS2 and SS3 occur, but not necessarily in the programmed priority order.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

10 UART

10.1 The RTRIS bit in the UARTRIS register is only set when the interrupt is enabled

Description:

The RTRIS (UART Receive Time-Out Raw Interrupt Status) bit in the **UART Raw Interrupt Status (UARTRIS)** register should be set when a receive time out occurs, regardless of the state of the RTIM enable bit in the **UART Interrupt Mask (UARTIM)** register. However, currently the RTIM bit must be set in order for the RTRIS bit to be set when a receive time out occurs.

Workaround:

For applications that require polled operation, the RTIM bit can be set while the UART interrupt is disabled in the NVIC using the IntDisable(n) function in the StellarisWare Peripheral Driver Library, where n is 21, 22, or 49 depending on whether UART0, UART1 or UART2 is used. With this configuration, software can poll the RTRIS bit, but the interrupt is not reported to the NVIC.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

10.2 LIN mode Sync Break does not have the correct length

Description:

When operating as a LIN master, the microcontroller provides a Sync Break of the length that is programmed in the BLEN field in the **UART LIN Control (UARTLCTL)** register. However, the actual Sync Break length is 1 less than what is programmed in the BLEN field as shown in Table 3 on page 30.

Table 3. SyncBreak Length

BLEN Encoding	Data Sheet Value	Actual Value
0x0	13T bits	12T bits
0x1	14T bits	13T bits
0x2	15T bits	14T bits
0x3	16T bits	15T bits

Workaround:

Adjust the BLEN encoding to correspond to the actual Sync Break required.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

10.3 When UART LIN or SIR mode is enabled, µDMA burst transfer does not occur

Description:

If the LIN or the IrDA Serial Infrared (SIR) mode is enabled in the UART peripheral and the uDMA UARTn RX or UARTn TX channel is configured to do a burst transfer, the burst data transfer does not occur.

Workaround:

Clear the SETn bit in the **DMA Channel Useburst Set (DMAUSEBURSTSET)** register to have the uDMA UART channel respond to single or burst requests to ensure that the data transfer occurs.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

10.4 UART transfers fail at certain system clock frequency and baud rate combinations

Description:

UART data transfers using the TXRIS and RXRIS interrupt bits and FIFOs fail for certain combinations of the system clock frequency and baud rate.

System Clock Freq [MHz]	32	24	16	10	8	5	4	2	1
Failing Baud Rate [bps]	<460800	<460800	<230400	<460800	<115200	<230400	<57600	<38400	<19200

Workaround:

Use a system clock frequency above 32MHz if using the UART with the raw interrupt status bits or use µDMA UART data transfers instead of the TXRIS and RXRIS bits. When using µDMA UART data transfers, there are no system clock frequency and baud rate conflicts.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

11 SSI

11.1 Freescale SPI Mode at low SSIClk frequencies can yield data corruption

Description:

Data transmitted by the SPI slave may be corrupted when using Freescale SPI Mode 0 at an SSIClk frequency between 0.5 MHz to 1.1 MHz and a system clock frequency of 33 MHz or lower.

Workaround:

Operate the Freescale SPI Mode 0 at an SSIClk frequency above 1.1 MHz and use a system clock frequency above 33 MHz or use a different mode.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

12 USB

12.1 USB paired JK jitter compliance test requires automatic waiver

Description:

The USB compliance test results in a Paired JK jitter failure.

Workaround:

This failure comes with an automatic waiver from usb.org so certification can still be granted.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

12.2 USB low speed crossover voltage compliance test requires automatic waiver

Description:

The USB compliance test results in a crossover voltage range failure when talking to low speed devices.

Workaround:

This failure comes with an automatic waiver from usb.org so certification can still be granted.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

12.3 MCU may fail USB certification if the EPI module is operating

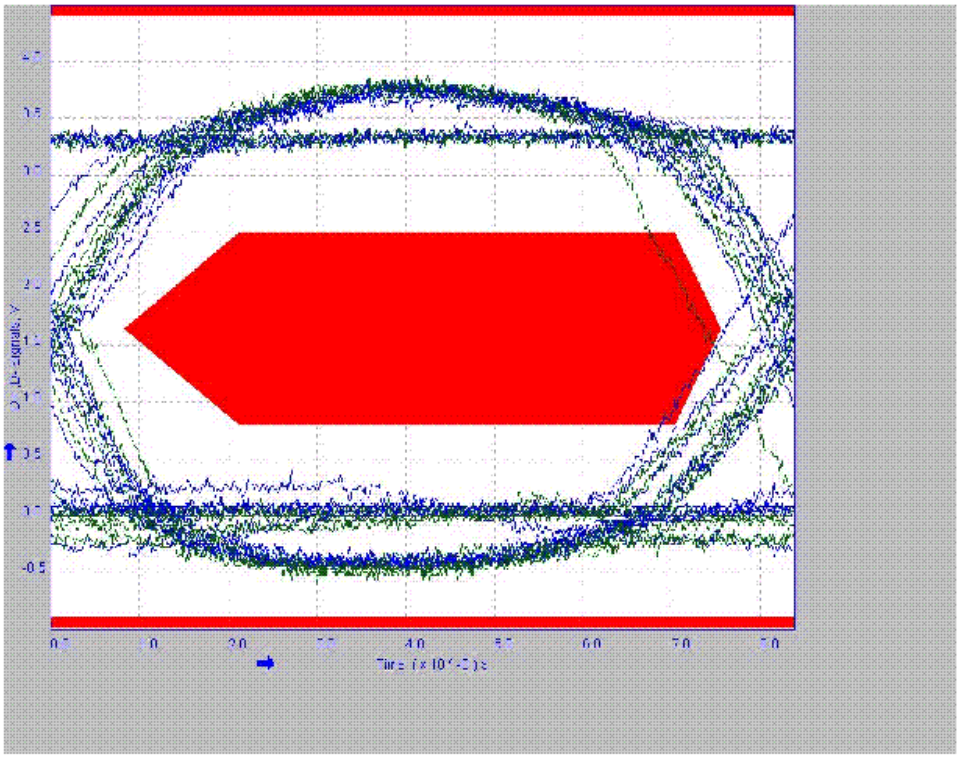
Description:

If the EPI module is operating, the USB interface may fail USB certification. Failures have been seen for the eye diagram and jitter (see Figure 4 on page 33). Because of these issues, there is a potential for data corruption on the USB interface when using the USB and EPI at the same time. The risk of data corruption is small, but is dependent on the system design.

The USB hardware senses bit errors in the CRC check for control, interrupt, and bulk transfers. If an error occurs, the host hardware requests a resend of the packet up to three times. The application software could be written to address this error further if needed.

Figure 4. Example of USB Certification Failure

- Signal eye:
  Eye Diagram Test fails



- EOP width: 169.0995ns
  EOP width passes
- Receivers: reliable operation on tier Tier 6
  Receivers pass
- Measured Signalling Rate: 11.92707Mbps
  signal rate conditionally passes
- Crossover voltage range: 1.546667 V to 1.680000 V
  Mean crossover = 1.615889 V
  First crossover at 1.660000 V(11 other differential crossovers checked)
  crossover voltages pass
- Consecutive jitter range: -165.1885ns to 1.811468ns, RMS jitter 52.27256ns
  Paired JK jitter range: 752.3810ps to 2.871429ns, RMS jitter 1.821542ns
  Paired KJ jitter range: 1.185714ns to 2.168571ns, RMS jitter 1.695397ns
  jitter fails

USB certification can be attained if an application does not require the USB and the EPI to be operating simultaneously. Customers who do not intend to pursue USB certification should determine if their application can handle the resulting small amount of error.

Workaround:

None.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

12.4 Special considerations for PB1

Description:

When using PB1 as a GPIO, special considerations are required due to issue “PB1 has permanent internal pull-up resistance” on page 18.

Workaround:

The DEVMODOTG and DEVMOD bits in the **USB General-Purpose Control and Status (USBGPCS)** register can be used to configure the USB controller to operate only in Host mode or Device mode and allowing PB0 and PB1 to be used as GPIOs. If both the DEVMODOTG and DEVMOD bits are set, indicating Device mode, the USB VBUS signal must be monitored using a GPIO as an input to detect connect and disconnect. This monitoring must be done with a GPIO other than PB1, because PB1 is not 5-V tolerant. Note that this erratum does not affect devices operating in OTG mode. The USB0VBUS signal operates as specified.

In addition, if the USB functionality is not used on the device, in order to be able to use PB1 as a GPIO, the user application must enable the USB module in the **RCGC2** register, set the DEVMODOTG bit, and then disable the USB module again. The restrictions detailed in issue “PB1 has permanent internal pull-up resistance” on page 18 still apply.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

12.5 Cannot communicate with a low-speed Device through a hub

Description:

When the USB controller is operating as a Host and a low-speed packet is sent to a Device through a hub, the subsequent Start-of-Frame is corrupted. After a period of time, this corruption causes the USB controller to lose synchronization with the hub, resulting in data corruption.

Workaround:

None.

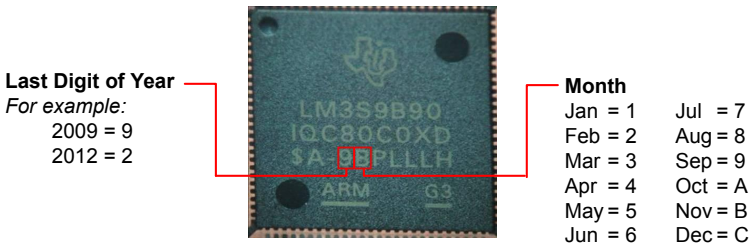
Silicon Revision Affected:

C5

Fixed:

Fixed on devices with date codes of 1A (October 2011) or later. In addition, the system clock on the MCU must be at least 30 MHz.

Note: To determine the date code of your part, look at the first two characters following the dash on the third line of the part markings (highlighted in red in the following figure). The first number after the dash indicates the last decimal digit of the year. The second character indicates the month. Therefore, the following example shows a date code of 9B which indicates November 2009.



12.6 USB0DM may be driven after reset

Description:

If the microcontroller is reset while the USB device is connected to an upstream port with the SOFTCONN bit set in the **USB Power (USBPOWER)** register, the USB0DM signal is driven to 2 V for 66 µs after the microcontroller comes out of reset. This activity can appear to be unsolicited traffic to the upstream port. This traffic is generally ignored, but may cause unexpected behavior from the upstream host controller.

Workaround:

If the system can determine that a reset is about to occur, disconnect the USB peripheral by clearing the SOFTCONN bit in the **USB Power (USBPOWER)** register prior to resetting the device. If the microcontroller reset is asynchronous, there is no workaround.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

13 PWM

13.1 PWM fault latch does not operate correctly

Description:

If the LATCH bit is set in th **PWMnCTL** register, the PWM fault condition should be latched until the INTFAULTn bit in the **PWMISC** register is cleared. However, the PWM fault signal is not correctly latched and the PWM resumes programmed signalling after the fault condition is removed, regardless of whether the INTFAULTn bit is cleared.

Workaround:

Software can effectively address this issue with the addition of a few register writes in the ISR.

1. The **PWMnMINFLTPER** register can be used to ensure that the fault is asserted for a long enough period such that the ISR can be called to implement the workaround.
2. The PWM output can be disabled manually using the PWMnEN bit in the **PWMENABLE** register.
3. Software can perform computations to determine if the PWM can be restarted.
4. The INTFAULTn bit in the **PWMISC** is cleared by writing a 1 to it.

5. The PWM output can be manually re-enabled using the PWMnEN bit in the **PWMENABLE** register.

Note that when using this workaround, the PWM output is disabled manually, which means it does not go to the "pre-programmed" state from various fault registers but instead goes to 0.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

14 Electrical Characteristics

14.1 First two ADC samples from the internal temperature sensor must be ignored

Description:

The analog source resistance (Rs) to the ADC from the internal temperature sensor exceeds the specified amount of 500Ω. This causes a settling time requirement that is longer than the sampling interval to the converter.

Workaround:

Three consecutive samples from the same channel must be taken to accurately sample the internal temperature sensor using the ADC. The first two consecutive samples should be discarded and the third sample can be kept. These consecutive samples cannot be interrupted by sampling another channel.

Silicon Revision Affected:

C5

Fixed:

Not yet fixed.

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