LMP7701/LMP7702/LMP7704 Precision, CMOS Input, RRIO, Wide Supply Range Amplifiers

Check for Samples: LMP7701, LMP7702, LMP7704

FEATURES

- **Unless Otherwise Noted, Typical Values at V_S = 5V**
  - **Input Offset Voltage (LMP7701): ±200 µV (max)**
  - **Input Offset Voltage (LMP7702/LMP7704): ±220 µV (max)**
  - **Input Bias Current: ±200 fA**
  - **Input Bias Current: ±200 fA**
  - **Input Voltage Noise: 9 nV/√Hz**
  - **CMRR: 130 dB**
  - **Open Loop Gain: 130 dB**
  - **Temperature Range: −40°C to 125°C**
  - **Unity Gain Bandwidth: 2.5 MHz**
  - **Supply Current (LMP7701): 715 µA**
  - **Supply Current (LMP7702): 1.5 mA**
  - **Supply Current (LMP7704): 2.9 mA**
  - **Supply Voltage Range: 2.7V to 12V**
  - **Rail-to-Rail Input and Output**

APPLICATIONS

- **High Impedance Sensor Interface**
- **Battery Powered Instrumentation**
- **High Gain Amplifiers**
- **DAC Buffer**
- **Instrumentation Amplifier**
- **Active Filters**

DESCRIPTION

The LMP7701/LMP7702/LMP7704 are single, dual, and quad low offset voltage, rail-to-rail input and output precision amplifiers each with a CMOS input stage and a wide supply voltage range. The LMP7701/LMP7702/LMP7704 are part of the LMP™ precision amplifier family and are ideal for sensor interface and other instrumentation applications.

The specified low offset voltage of less than ±200 µV along with the specified low input bias current of less than ±1 pA make the LMP7701 ideal for precision applications. The LMP7701/LMP7702/LMP7704 are built utilizing VIP50 technology, which allows the combination of a CMOS input stage and a 12V common mode and supply voltage range. This makes the LMP7701/LMP7702/LMP7704 great choices in many applications where conventional CMOS parts cannot operate under the desired voltage conditions.

The LMP7701/LMP7702/LMP7704 each have a rail-to-rail input stage that significantly reduces the CMRR glitch commonly associated with rail-to-rail input amplifiers. This is achieved by trimming both sides of the complimentary input stage, thereby reducing the difference between the NMOS and PMOS offsets. The output of the LMP7701/LMP7702/LMP7704 swings within 40 mV of either rail to maximize the signal dynamic range in applications requiring low supply voltage.

The LMP7701 is offered in the space saving 5-Pin SOT-23 and 8-Pin SOIC package. The LMP7702 is offered in the 8-Pin SOIC and 8-Pin VSSOP package. The quad LMP7704 is offered in the 14-Pin SOIC and 14-Pin TSSOP package. These small packages are ideal solutions for area constrained PC boards and portable electronics.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL APPLICATION

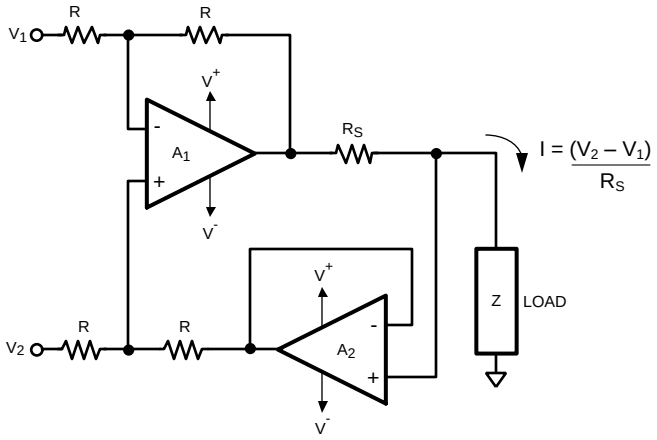


Figure 1. Precision Current Source

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	Human Body Model	2000V
	Machine Model	200V
	Charge-Device Model	1000V
V_{IN} Differential		±300 mV
Supply Voltage ($V_S = V^+ – V^–$)		13.2V
Voltage at Input/Output Pins		V^++ 0.3V, $V^–$ − 0.3V
Input Current		10 mA
Storage Temperature Range		−65°C to +150°C
Junction Temperature (4)		+150°C
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering Lead Temp. (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings (1)

Temperature Range (2)		−40°C to +125°C
Supply Voltage ($V_S = V^+ – V^-$)		2.7V to 12V
Package Thermal Resistance (θ_{JA} (2))	5-Pin SOT-23	265°C/W
	8-Pin SOIC	190°C/W
	8-Pin VSSOP	235°C/W
	14-Pin SOIC	145°C/W
	14-Pin TSSOP	122°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

3V Electrical Characteristics (1)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 3V, V^- = 0V, $V_{CM} = V^+/2$, and R_L > 10 kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	LMP7701		±37	±200 **±500**	µV
		LMP7702/LMP7704		±56	±220 **±520**	
TCV_{OS}	Input Offset Voltage Temperature Drift	(4)		±1	**±5**	µV/°C
I_B	Input Bias Current	(4) (5) −40°C ≤ T_A ≤ 85°C		±0.2	±1 **±50**	pA
		(4) (5) −40°C ≤ T_A ≤ 125°C		±0.2	±1 **±400**	
I_{OS}	Input Offset Current			40		fA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3V LMP7701	86 **80**	130		dB
		0V ≤ V_{CM} ≤ 3V LMP7702/LMP7704	84 **78**	130		
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 12V, Vo = $V^+/2$	86 **82**	98		dB
CMVR	Common Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 77 dB	–0.2 **–0.2**		3.2 **3.2**	V
A_{VOL}	Open Loop Voltage Gain	R_L = 2 kΩ (LMP7701) V_O = 0.3V to 2.7V	100 **96**	114		dB
		R_L = 2 kΩ (LMP7702/LMP7704) V_O = 0.3V to 2.7V	100 **94**	114		
		R_L = 10 kΩ V_O = 0.2V to 2.8V	100 **96**	124		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) This parameter is specified by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.

3V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = V^+/2, and R_L > 10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min (2)	Typ (3)	Max (2)	Units
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to V^+/2 LMP7701		40	80 **120**	mV from V^+
		R_L = 2 kΩ to V^+/2 LMP7702/LMP7704		40	80 **150**	
		R_L = 10 kΩ to V^+/2 LMP7701		30	40 **60**	
		R_L = 10 kΩ to V^+/2 LMP7702/LMP7704		35	50 **100**	
	Output Voltage Swing Low	R_L = 2 kΩ to V^+/2 LMP7701		40	60 **80**	mV
		R_L = 2 kΩ to V^+/2 LMP7702/LMP7704		45	100 **170**	
		R_L = 10 kΩ to V^+/2 LMP7701		20	40 **50**	
		R_L = 10 kΩ to V^+/2 LMP7702/LMP7704		20	50 **90**	
I_{OUT}	Output Current (6) (7)	Sourcing V_O = V^+/2 V_{IN} = 100 mV	25 **15**	42		mA
		Sinking V_O = V^+/2 V_{IN} = −100 mV (LMP7701)	25 **20**	42		
		Sinking V_O = V^+/2 V_{IN} = −100 mV (LMP7702/LMP7704)	25 **15**	42		
I_S	Supply Current	LMP7701		0.670	1.0 **1.2**	mA
		LMP7702		1.4	1.8 **2.1**	
		LMP7704		2.9	3.5 **4.5**	
SR	Slew Rate (8)	A_V = +1, V_O = 2 V_{PP} 10% to 90%		0.9		V/µs
GBW	Gain Bandwidth			2.5		MHz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_L = 10 kΩ		0.02		%
e_n	Input Referred Voltage Noise Density	f = 1 kHz		9		nV/√Hz
i_n	Input Referred Current Noise Density	f = 100 kHz		1		fA/√Hz

(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.
(7) The short circuit test is a momentary test.
(8) The number specified is the slower of positive and negative slew rates.

5V Electrical Characteristics (1)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, and R_L > 10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	LMP7701		±37	±200 **±500**	µV
		LMP7702/LMP7704		±32	±220 **±520**	
TCV_{OS}	Input Offset Voltage Temperature Drift	(4)		±1	**±5**	µV/°C
I_B	Input Bias Current	(4) (5) −40°C ≤ T_A ≤ 85°C		±0.2	±1 **±50**	pA
		(4) (5) −40°C ≤ T_A ≤ 125°C		±0.2	±1 **±400**	
I_{OS}	Input Offset Current			40		fA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 5V LMP7701	88 **83**	130		dB
		0V ≤ V_{CM} ≤ 5V LMP7702/LMP7704	86 **81**	130		
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 12V, V_O = V^+/2	86 **82**	100		dB
CMVR	Common Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB	–0.2 **–0.2**		5.2 **5.2**	V
A_{VOL}	Open Loop Voltage Gain	R_L = 2 kΩ (LMP7701) V_O = 0.3V to 4.7V	100 **96**	119		dB
		R_L = 2 kΩ (LMP7702/LMP7704) V_O = 0.3V to 4.7V	100 **94**	119		
		R_L = 10 kΩ V_O = 0.2V to 4.8V	100 **96**	130		
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to V^+/2 LMP7701		60	110 **130**	mV from V^+
		R_L = 2 kΩ to V^+/2 LMP7702/LMP7704		60	120 **200**	
		R_L = 10 kΩ to V^+/2 LMP7701		40	50 **70**	
		R_L = 10 kΩ to V^+/2 LMP7702/LMP7704		40	60 **120**	
	Output Voltage Swing Low	R_L = 2 kΩ to V^+/2 LMP7701		50	80 **90**	mV
		R_L = 2 kΩ to V^+/2 LMP7702/LMP7704		50	120 **190**	
		R_L = 10 kΩ to V^+/2 LMP7701		30	40 **50**	
		R_L = 10 kΩ to V^+/2 LMP7702/LMP7704		30	50 **100**	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) This parameter is specified by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.

5V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, and R_L > 10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min (2)	Typ (3)	Max (2)	Units
I_{OUT}	Output Current (6) (7)	Sourcing V_O = V^+/2 V_{IN} = 100 mV (LMP7701)	40 **28**	66		mA
		Sourcing V_O = V^+/2 V_{IN} = 100 mV (LMP7702/LMP7704)	38 **25**	66		
		Sinking V_O = V^+/2 V_{IN} = −100 mV (LMP7701)	40 **28**	76		
		Sinking V_O = V^+/2 V_{IN} = −100 mV (LMP7702/LMP7704)	40 **23**	76		
I_S	Supply Current	LMP7701		0.715	1.0 **1.2**	mA
		LMP7702		1.5	1.9 **2.2**	
		LMP7704		2.9	3.7 **4.6**	
SR	Slew Rate (8)	A_V = +1, V_O = 4 V_{PP} 10% to 90%		1.0		V/µs
GBW	Gain Bandwidth			2.5		MHz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_L = 10 kΩ		0.02		%
e_n	Input Referred Voltage Noise Density	f = 1 kHz		9		nV/√Hz
i_n	Input Referred Current Noise Density	f = 100 kHz		1		fA/√Hz

(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.
(7) The short circuit test is a momentary test.
(8) The number specified is the slower of positive and negative slew rates.

±5V Electrical Characteristics (1)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5V, V^- = −5V, V_{CM} = 0V, and R_L > 10 kΩ to 0V. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	LMP7701		±37	±200 **±500**	µV
		LMP7702/LMP7704		±37	±220 **±520**	
TCV_{OS}	Input Offset Voltage Temperature Drift	(4)		±1	**±5**	µV/°C
I_B	Input Bias Current	(4) (5) −40°C ≤ T_A ≤ 85°C		±0.2	1 **±50**	pA
		(4) (5) −40°C ≤ T_A ≤ 125°C		±0.2	1 **±400**	
I_{OS}	Input Offset Current			40		fA
CMRR	Common Mode Rejection Ratio	−5V ≤ V_{CM} ≤ 5V LMP7701	92 **88**	138		dB
		−5V ≤ V_{CM} ≤ 5V LMP7702/LMP7704	90 **86**	138		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) This parameter is specified by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.

±5V Electrical Characteristics [1] (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5V, V^- = −5V, V_{CM} = 0V, and R_L > 10 kΩ to 0V. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min [2]	Typ [3]	Max [2]	Units
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 12V, V_O = 0V	86 **82**	98		dB
CMVR	Common Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB	−5.2 **−5.2**		5.2 **5.2**	V
A_{VOL}	Open Loop Voltage Gain	R_L = 2 kΩ (LMP7701) V_O = −4.7V to 4.7V	100 **98**	121		dB
		R_L = 2 kΩ (LMP7702/LMP7704) V_O = −4.7V to 4.7V	100 **94**	121		
		R_L = 10 kΩ (LMP7701) V_O = −4.8V to 4.8V	100 **98**	134		
		R_L = 10 kΩ (LMP7702/LMP7704) V_O = −4.8V to 4.8V	100 **97**	134		
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to 0V LMP7701		90	150 **170**	mV from V^+
		R_L = 2 kΩ to 0V LMP7702/LMP7704		90	180 **290**	
		R_L = 10 kΩ to 0V LMP7701		40	80 **100**	
		R_L = 10 kΩ to 0V LMP7702/LMP7704		40	80 **150**	
	Output Voltage Swing Low	R_L = 2 kΩ to 0V LMP7701		90	130 **150**	mV from V^-
		R_L = 2 kΩ to 0V LMP7702/LMP7704		90	180 **290**	
		R_L = 10 kΩ to 0V LMP7701		40	50 **60**	
		R_L = 10 kΩ to 0V LMP7702/LMP7704		40	60 **110**	
I_{OUT}	Output Current [6] [7]	Sourcing V_O = 0V V_{IN} = 100 mV (LMP7701)	50 **35**	86		mA
		Sourcing V_O = 0V V_{IN} = 100 mV (LMP7702/LMP7704)	48 **33**	86		
		Sinking V_O = 0V V_{IN} = −100 mV	50 **35**	84		
I_S	Supply Current	LMP7701		0.790	1.1 **1.3**	mA
		LMP7702		1.7	2.1 **2.5**	
		LMP7704		3.2	4.2 **5.0**	
SR	Slew Rate [8]	A_V = +1, V_O = 9 V_{PP} 10% to 90%		1.1		V/µs
GBW	Gain Bandwidth			2.5		MHz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_L = 10 kΩ		0.02		%
e_n	Input Referred Voltage Noise Density	f = 1 kHz		9		nV/√Hz
i_n	Input Referred Current Noise Density	f = 100 kHz		1		fA/√Hz

(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.
(7) The short circuit test is a momentary test.
(8) The number specified is the slower of positive and negative slew rates.

CONNECTION DIAGRAMS

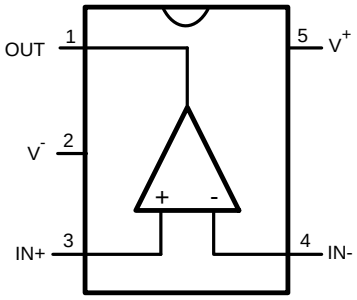


Figure 2. 5-Pin SOT-23 (LMP7701)
Top View

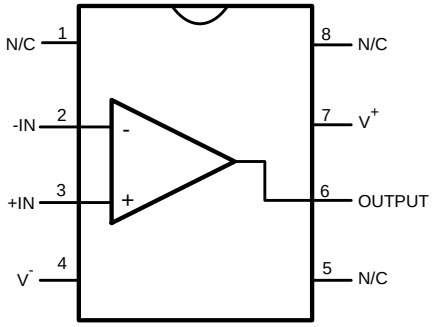


Figure 3. 8-Pin SOIC (LMP7701)
Top View

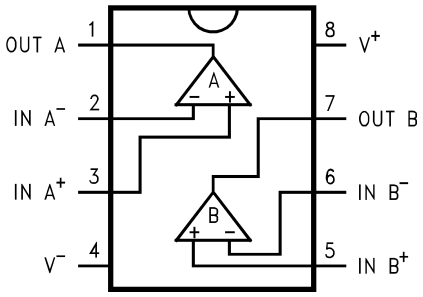


Figure 4. 8-Pin SOIC/VSSOP (LMP7702)
Top View

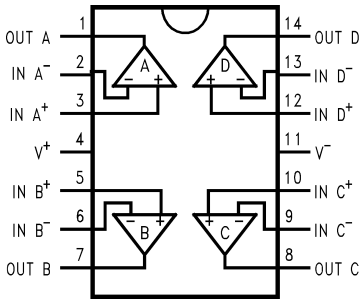


Figure 5. 14-Pin SOIC/TSSOP (LMP7704)
Top View

Typical Performance Characteristics

Unless otherwise noted: T_A = 25°C, V_{CM} = V_S/2, R_L > 10 kΩ.

Offset Voltage Distribution

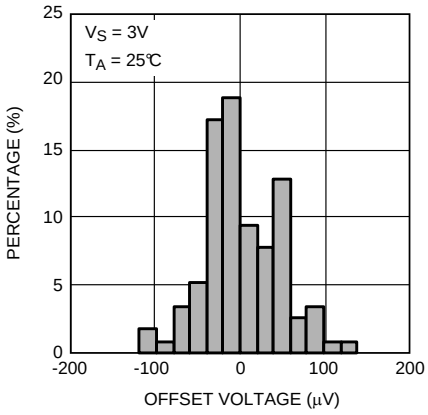


Figure 6.

TCV_{OS} Distribution

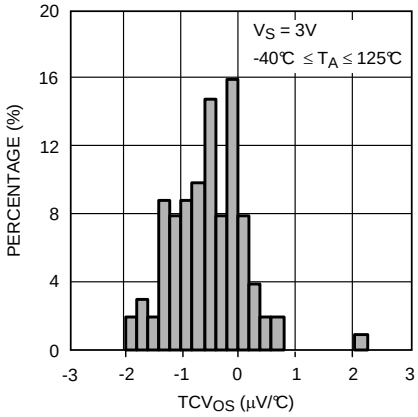


Figure 7.

Offset Voltage Distribution

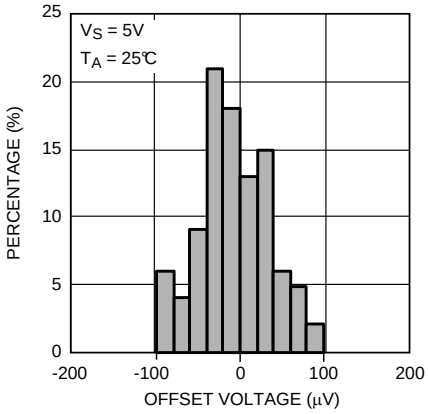


Figure 8.

TCV_{OS} Distribution

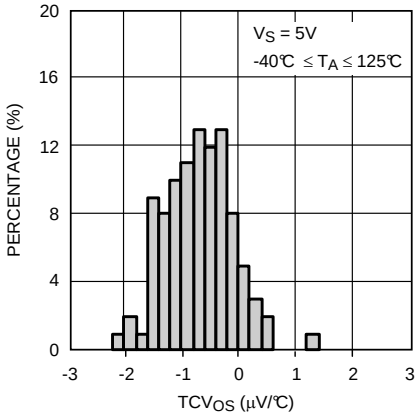


Figure 9.

Offset Voltage Distribution

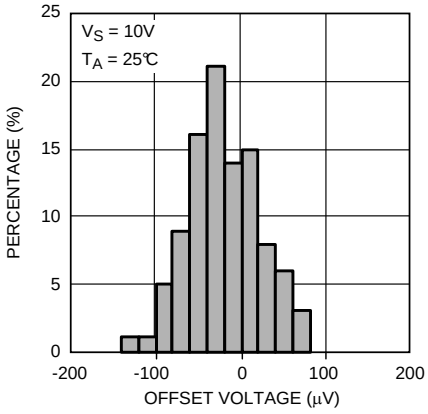


Figure 10.

TCV_{OS} Distribution

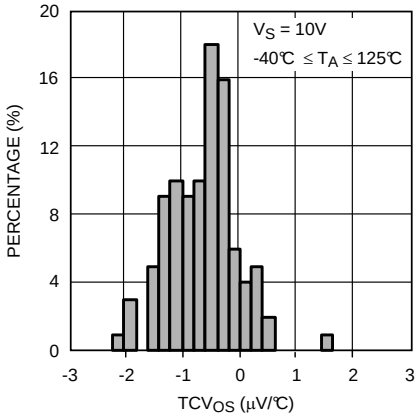


Figure 11.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, V_{CM} = V_S/2, R_L > 10 kΩ.

Offset Voltage vs. Temperature

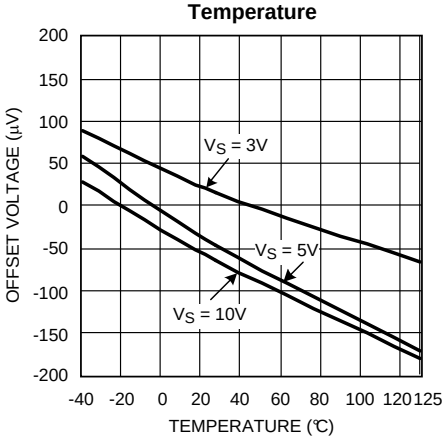


Figure 12.

CMRR vs. Frequency

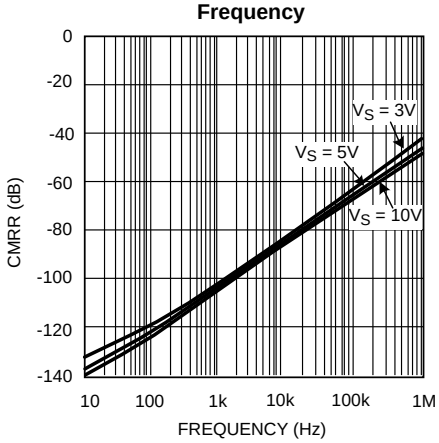


Figure 13.

Offset Voltage vs. Supply Voltage

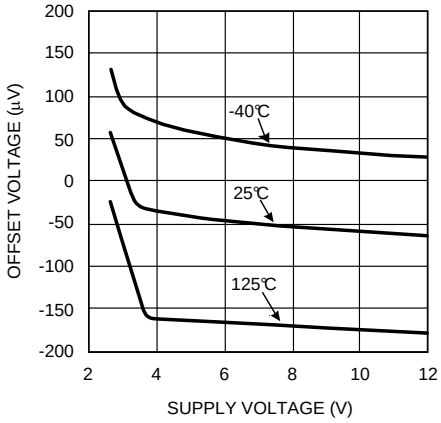


Figure 14.

Offset Voltage vs. V_{CM}

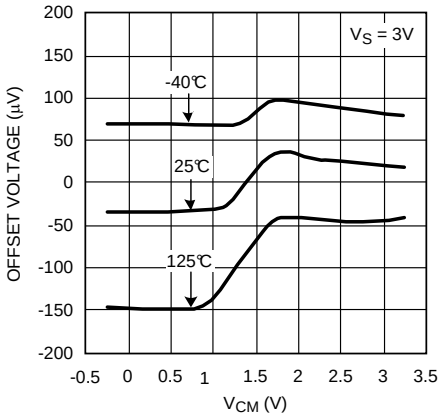


Figure 15.

Offset Voltage vs. V_{CM}

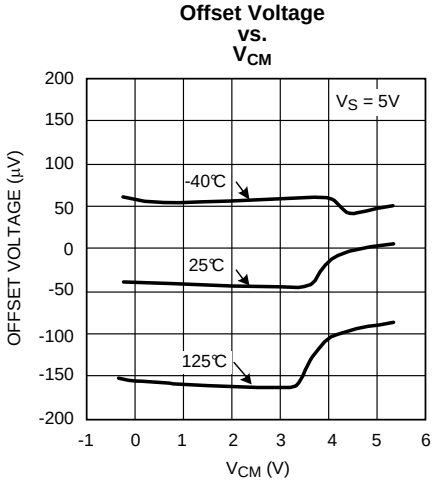


Figure 16.

Offset Voltage vs. V_{CM}

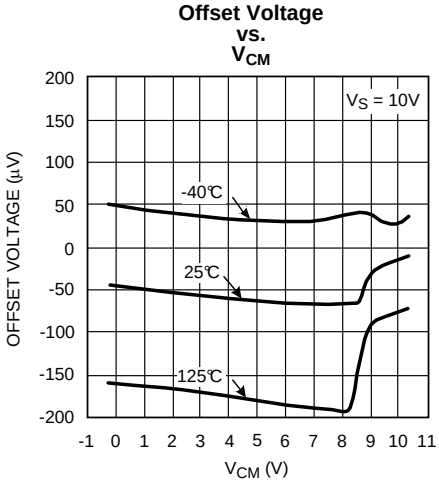


Figure 17.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, V_{CM} = V_S/2, R_L > 10 kΩ.

Input Bias Current vs. V_{CM}

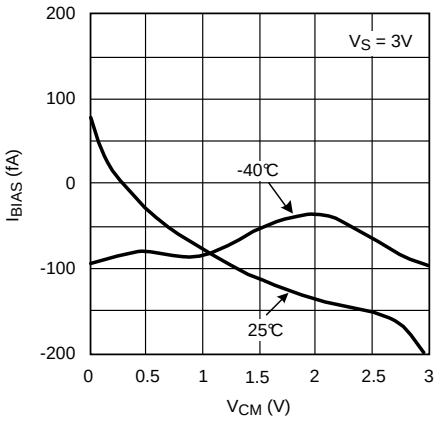


Figure 18.

Input Bias Current vs. V_{CM}

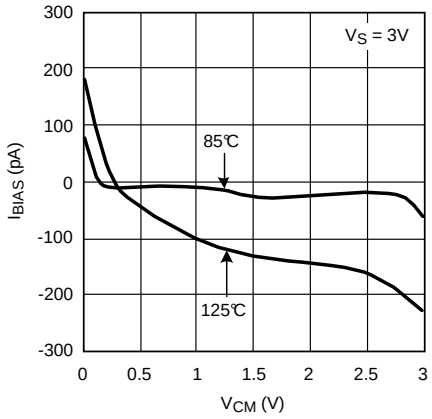


Figure 19.

Input Bias Current vs. V_{CM}

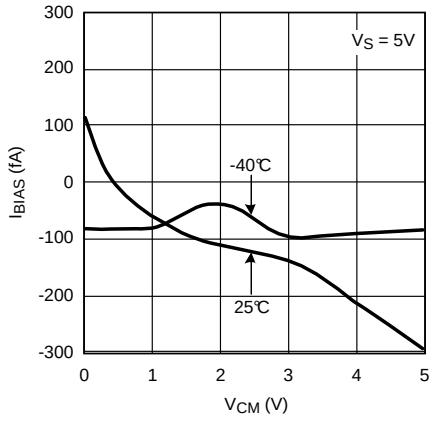


Figure 20.

Input Bias Current vs. V_{CM}

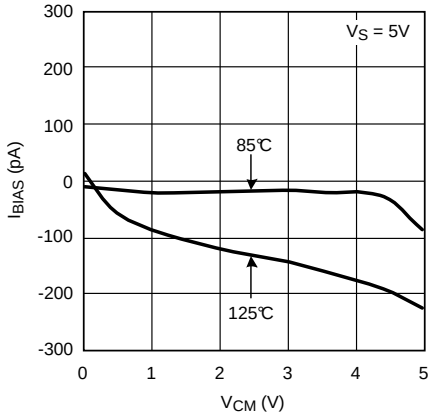


Figure 21.

Input Bias Current vs. V_{CM}

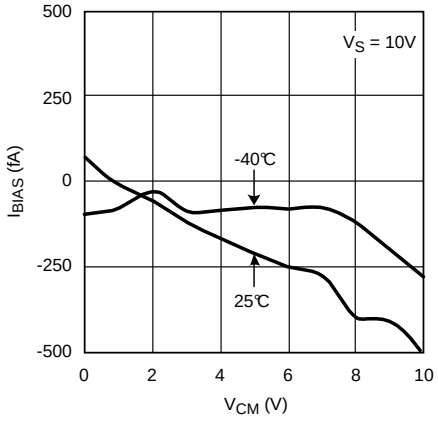


Figure 22.

Input Bias Current vs. V_{CM}

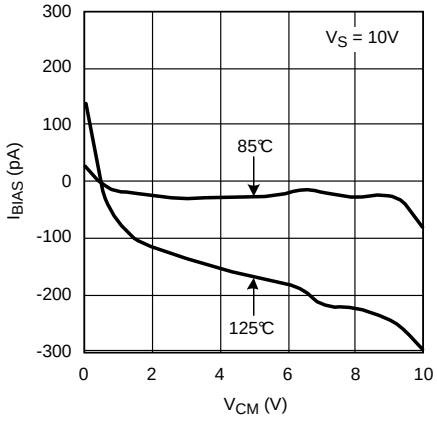


Figure 23.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, V_{CM} = V_S/2, R_L > 10 kΩ.

PSRR vs. Frequency

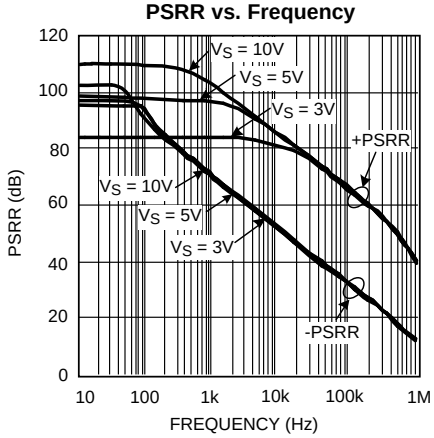


Figure 24.

Supply Current vs. Supply Voltage (Per Channel)

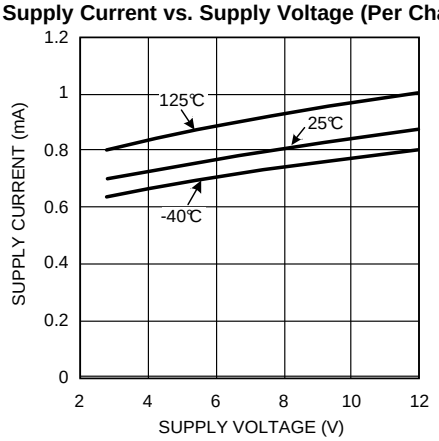


Figure 25.

Sinking Current vs. Supply Voltage

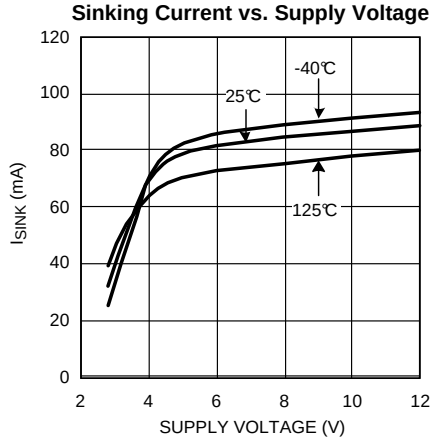


Figure 26.

Sourcing Current vs. Supply Voltage

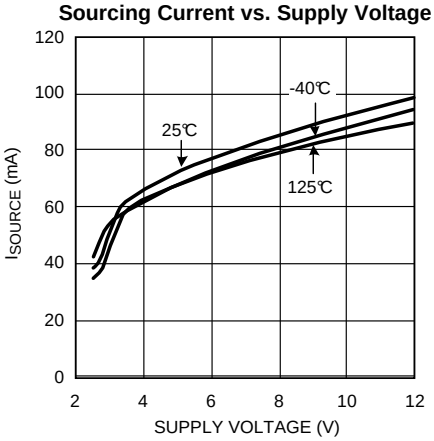


Figure 27.

Output Voltage vs. Output Current

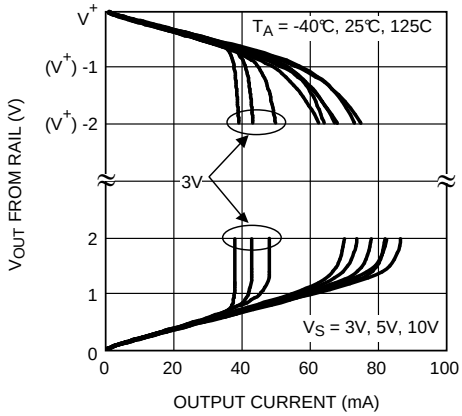


Figure 28.

Slew Rate vs. Supply Voltage

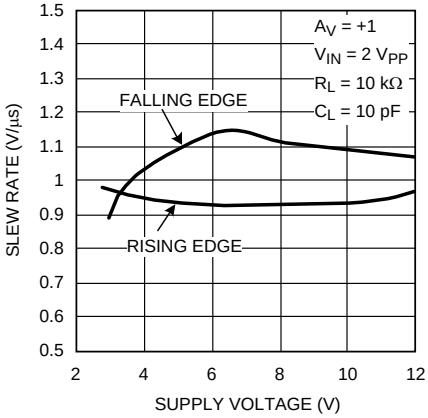


Figure 29.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, V_{CM} = V_S/2, R_L > 10 kΩ.

Open Loop Frequency Response

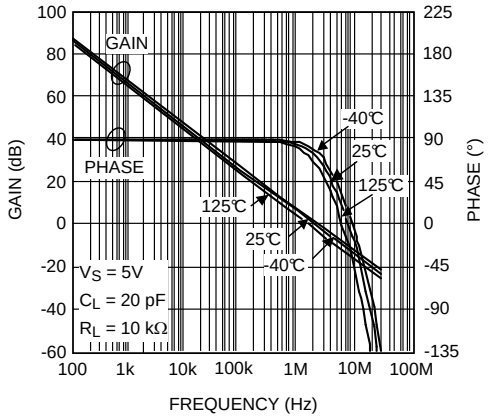


Figure 30.

Open Loop Frequency Response

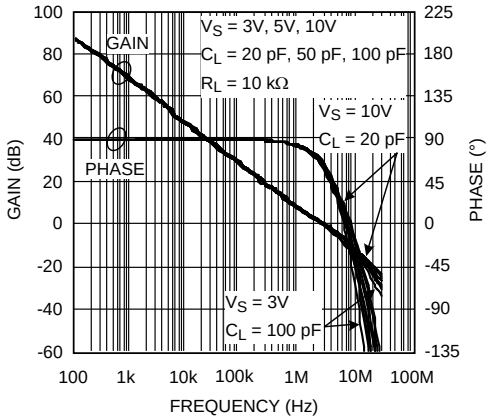


Figure 31.

Large Signal Step Response

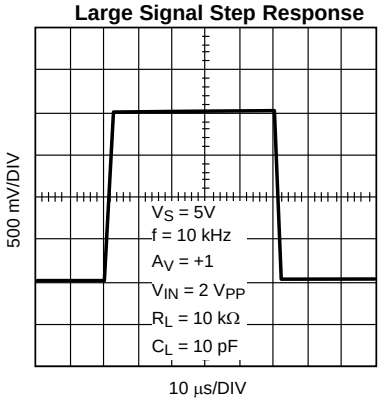


Figure 32.

Small Signal Step Response

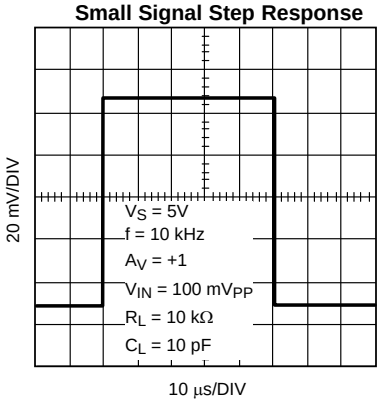


Figure 33.

Large Signal Step Response

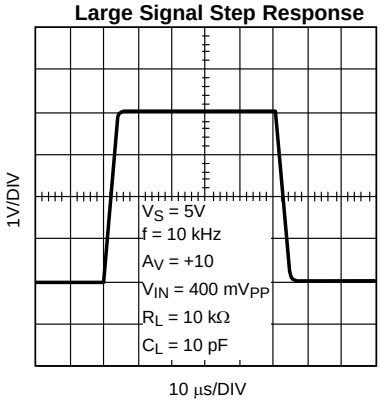


Figure 34.

Small Signal Step Response

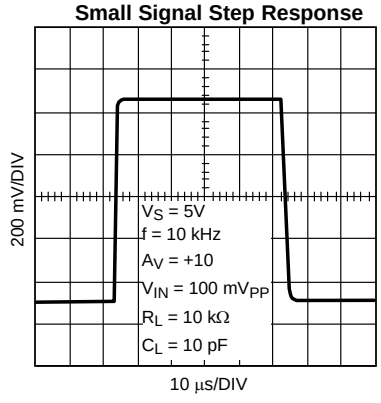


Figure 35.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, V_{CM} = V_S/2, R_L > 10 kΩ.

Input Voltage Noise vs. Frequency

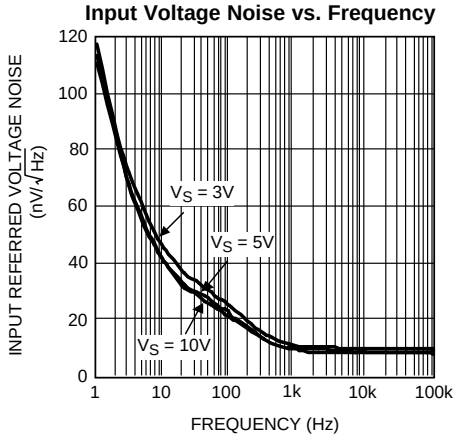


Figure 36.

Open Loop Gain vs. Output Voltage Swing

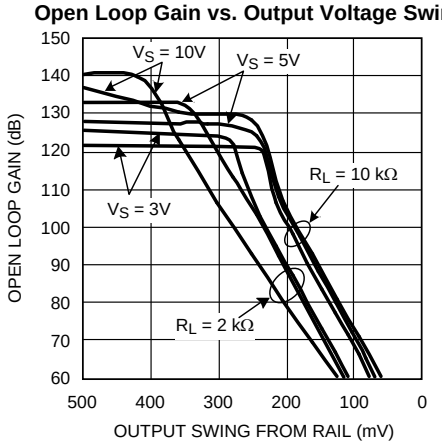


Figure 37.

Output Swing High vs. Supply Voltage

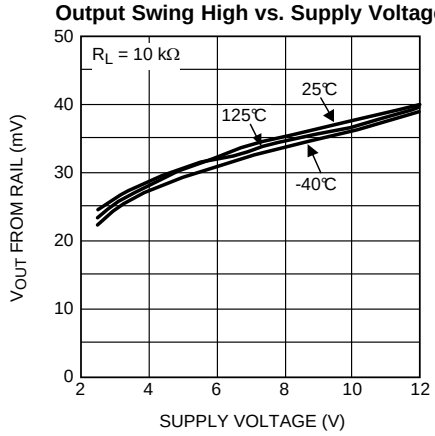


Figure 38.

Output Swing Low vs. Supply Voltage

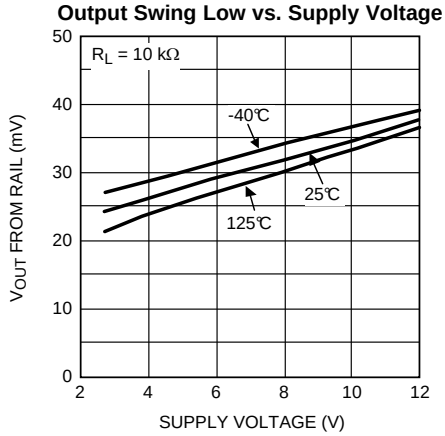


Figure 39.

Output Swing High vs. Supply Voltage

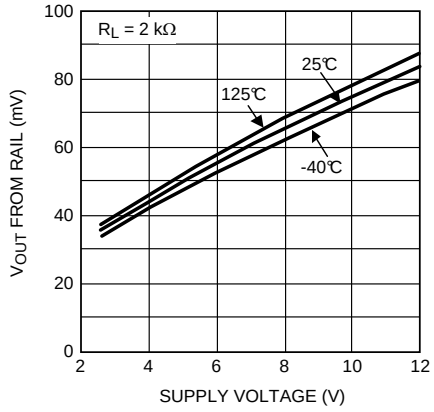


Figure 40.

Output Swing Low vs. Supply Voltage

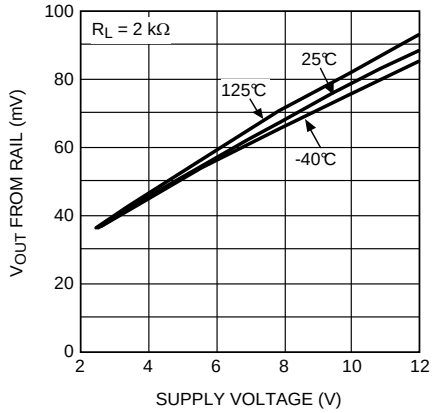


Figure 41.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, V_{CM} = V_S/2, R_L > 10 kΩ.

THD+N vs. Frequency

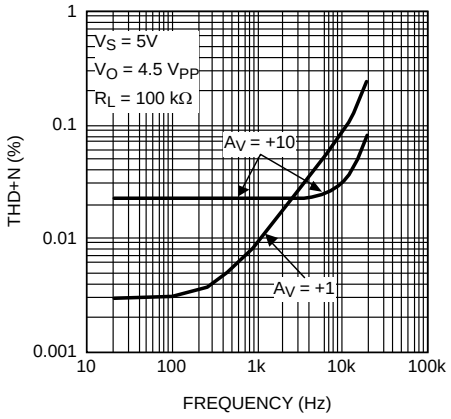


Figure 42.

THD+N vs. Output Voltage

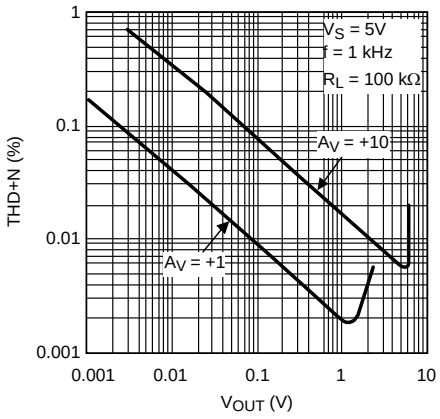


Figure 43.

Crosstalk Rejection Ratio vs. Frequency (LMP7702/LMP7704)

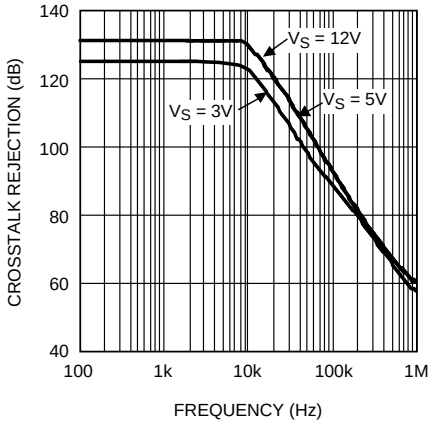


Figure 44.

APPLICATION INFORMATION

LMP7701/LMP7702/LMP7704

The LMP7701/LMP7702/LMP7704 are single, dual, and quad low offset voltage, rail-to-rail input and output precision amplifiers each with a CMOS input stage and wide supply voltage range of 2.7V to 12V. The LMP7701/LMP7702/LMP7704 have a very low input bias current of only ±200 fA at room temperature.

The wide supply voltage range of 2.7V to 12V over the extensive temperature range of −40°C to 125°C makes the LMP7701/LMP7702/LMP7704 excellent choices for low voltage precision applications with extensive temperature requirements.

The LMP7701/LMP7702/LMP7704 have only ±37 µV of typical input referred offset voltage and this offset is specified to be less than ±500 µV for the single and ±520 µV for the dual and quad, over temperature. This minimal offset voltage allows more accurate signal detection and amplification in precision applications.

The low input bias current of only ±200 fA along with the low input referred voltage noise of 9 nV/$\sqrt{Hz}$ gives the LMP7701/LMP7702/LMP7704 superiority for use in sensor applications. Lower levels of noise from the LMP7701/LMP7702/LMP7704 mean of better signal fidelity and a higher signal-to-noise ratio.

Texas Instruments is heavily committed to precision amplifiers and the market segment they serve. Technical support and extensive characterization data is available for sensitive applications or applications with a constrained error budget.

The LMP7701 is offered in the space saving 5-Pin SOT-23 and 8-Pin SOIC package. The LMP7702 comes in the 8-Pin SOIC and 8-Pin VSSOP package. The LMP7704 is offered in the 14-Pin SOIC and 14-Pin TSSOP package. These small packages are ideal solutions for area constrained PC boards and portable electronics.

CAPACITIVE LOAD

The LMP7701/LMP7702/LMP7704 can each be connected as a non-inverting unity gain follower. This configuration is the most sensitive to capacitive loading.

The combination of a capacitive load placed on the output of an amplifier along with the amplifier's output impedance creates a phase lag which in turn reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be either underdamped or it will oscillate.

In order to drive heavier capacitive loads, an isolation resistor, R_{ISO}, in Figure 45 should be used. By using this isolation resistor, the capacitive load is isolated from the amplifier's output, and hence, the pole caused by C_L is no longer in the feedback loop. The larger the value of R_{ISO}, the more stable the output voltage will be. If values of R_{ISO} are sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

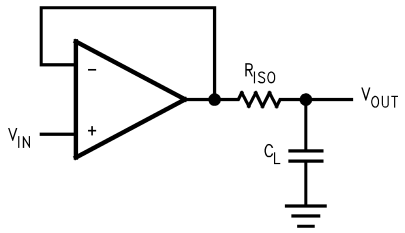


Figure 45. Isolating Capacitive Load

INPUT CAPACITANCE

CMOS input stages inherently have low input bias current and higher input referred voltage noise. The LMP7701/LMP7702/LMP7704 enhance this performance by having the low input bias current of only ±200 fA, as well as, a very low input referred voltage noise of 9 nV/$\sqrt{Hz}$. In order to achieve this a larger input stage has been used. This larger input stage increases the input capacitance of the LMP7701/LMP7702/ LMP7704. The typical value of this input capacitance, C_{IN}, for the LMP7701/LMP7702/LMP7704 is 25 pF. The input capacitance will interact with other impedances such as gain and feedback resistors, which are seen on the inputs of the

amplifier, to form a pole. This pole will have little or no effect on the output of the amplifier at low frequencies and DC conditions, but will play a bigger role as the frequency increases. At higher frequencies, the presence of this pole will decrease phase margin and will also cause gain peaking. In order to compensate for the input capacitance, care must be taken in choosing the feedback resistors. In addition to being selective in picking values for the feedback resistor, a capacitor can be added to the feedback path to increase stability.

The DC gain of the circuit shown in Figure 46 is simply $-R_2/R_1$.

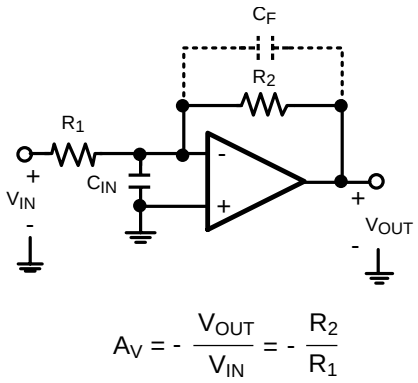


Figure 46. Compensating for Input Capacitance

For the time being, ignore C_F. The AC gain of the circuit in Figure 46 can be calculated as follows:

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{\left[1 + \frac{s}{\left(\frac{A_0 R_1}{R_1 + R_2}\right)} + \frac{s^2}{\left(\frac{A_0}{C_{IN} R_2}\right)}\right]}$$

This equation is rearranged to find the location of the two poles:

$$P_{1,2} = \frac{-1}{2C_{IN}}\left[\frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)^2 - \frac{4\,A_0 C_{IN}}{R_2}}\right] \quad (1)$$

As shown in Equation 1, as values of R_1 and R_2 are increased, the magnitude of the poles is reduced, which in turn decreases the bandwidth of the amplifier. Whenever possible, it is best to choose smaller feedback resistors. Figure 47 shows the effect of the feedback resistor on the bandwidth of the LMP7701/LMP7702/LMP7704.

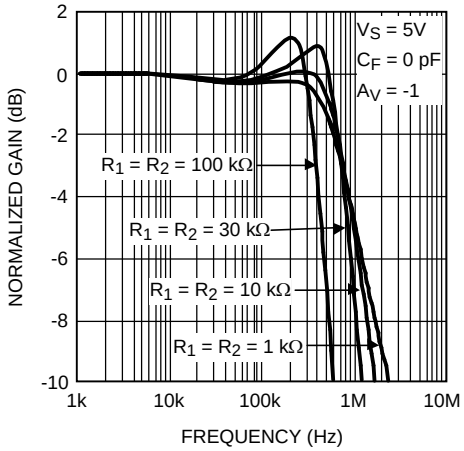


Figure 47. Closed Loop Gain vs. Frequency

Equation 1 has two poles. In most cases, it is the presence of pairs of poles that causes gain peaking. In order to eliminate this effect, the poles should be placed in Butterworth position, since poles in Butterworth position do not cause gain peaking. To achieve a Butterworth pair, the quantity under the square root in Equation 1 should be set to equal −1. Using this fact and the relation between R_1 and R_2, $R_2 = -A_V R_1$, the optimum value for R_1 can be found. This is shown in Equation 2. If R_1 is chosen to be larger than this optimum value, gain peaking will occur.

$$R_1 < \frac{(1 - A_V)^2}{2A_0A_VC_{IN}} \tag{2}$$

In Figure 46, C_F is added to compensate for input capacitance and to increase stability. Additionally, C_F reduces or eliminates the gain peaking that can be caused by having a larger feedback resistor. Figure 48 shows how C_F reduces gain peaking.

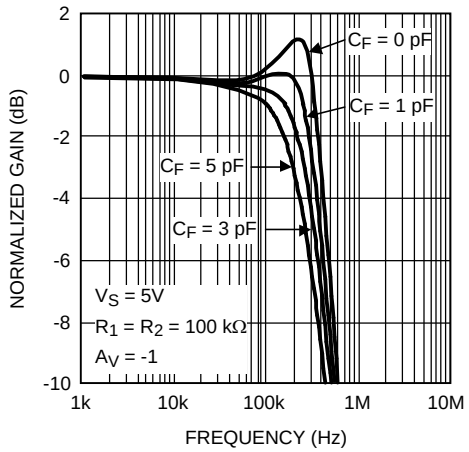


Figure 48. Closed Loop Gain vs. Frequency with Compensation

DIODES BETWEEN THE INPUTS

The LMP7701/LMP7702/LMP7704 have a set of anti-parallel diodes between the input pins, as shown in Figure 49. These diodes are present to protect the input stage of the amplifier. At the same time, they limit the amount of differential input voltage that is allowed on the input pins. A differential signal larger than one diode voltage drop might damage the diodes. The differential signal between the inputs needs to be limited to ±300 mV or the input current needs to be limited to ±10 mA.

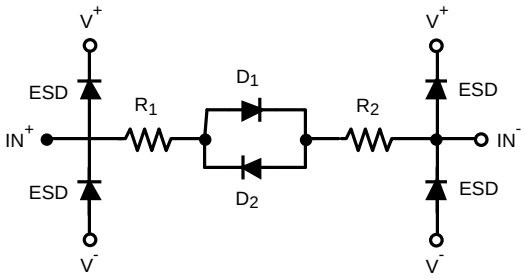


Figure 49. Input of LMP7701

PRECISION CURRENT SOURCE

The LMP7701/LMP7702/LMP7704 can each be used as a precision current source in many different applications. Figure 50 shows a typical precision current source. This circuit implements a precision voltage controlled current source. Amplifier A1 is a differential amplifier that uses the voltage drop across R_S as the feedback signal. Amplifier A2 is a buffer that eliminates the error current from the load side of the R_S resistor that would flow in the feedback resistor if it were connected to the load side of the R_S resistor. In general, the circuit is stable as long as the closed loop bandwidth of amplifier A2 is greater then the closed loop bandwidth of amplifier A1. Note that if A1 and A2 are the same type of amplifiers, then the feedback around A1 will reduce its bandwidth compared to A2.

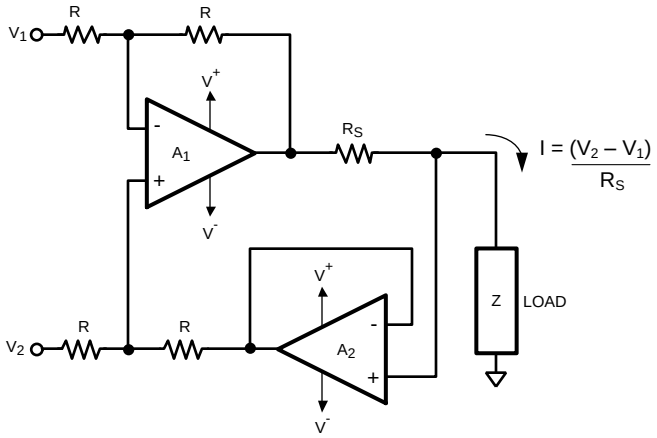


Figure 50. Precision Current Source

The equation for output current can be derived as follows:

$$\frac{V_2R}{R+R} + \frac{(V_0 - IR_S)R}{R+R} = \frac{V_1R}{R+R} + \frac{V_0R}{R+R}$$

Solving for the current I results in the following equation:

$$I = \frac{V_2 - V_1}{R_S}$$

LOW INPUT VOLTAGE NOISE

The LMP7701/LMP7702/LMP7704 have the very low input voltage noise of 9 nV/$\sqrt{Hz}$. This input voltage noise can be further reduced by placing N amplifiers in parallel as shown in Figure 51. The total voltage noise on the output of this circuit is divided by the square root of the number of amplifiers used in this parallel combination. This is because each individual amplifier acts as an independent noise source, and the average noise of independent sources is the quadrature sum of the independent sources divided by the number of sources. For N identical amplifiers, this means:

$$\text{REDUCED INPUT VOLTAGE NOISE} = \frac{1}{N}\sqrt{e_{n1}^2 + e_{n2}^2 + \cdots + e_{nN}^2}$$

$$= \frac{1}{N}\sqrt{Ne_n^2} = \frac{\sqrt{N}}{N}\, e_n$$

$$= \frac{1}{\sqrt{N}}\, e_n$$

Figure 51 shows a schematic of this input voltage noise reduction circuit. Typical resistor values are:

R_G = 10Ω, R_F = 1 kΩ, and R_O = 1 kΩ.

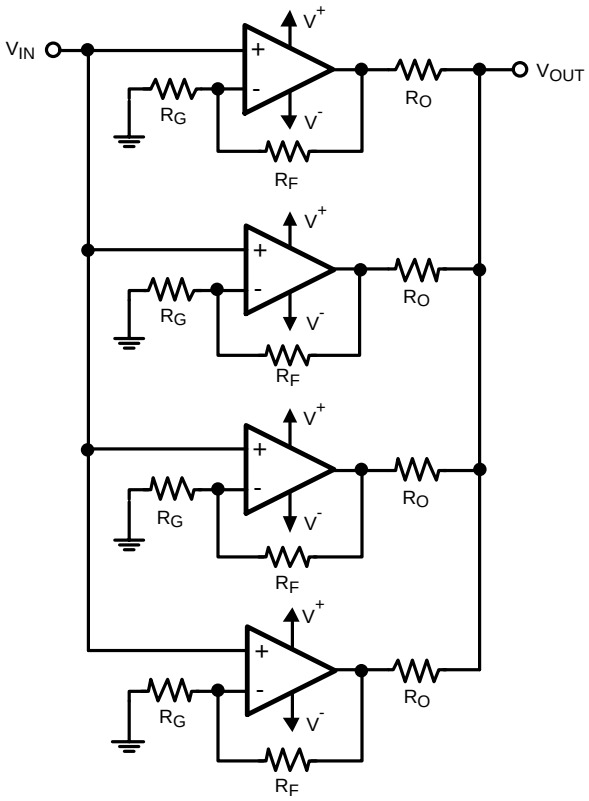


Figure 51. Noise Reduction Circuit

TOTAL NOISE CONTRIBUTION

The LMP7701/LMP7702/LMP7704 have very low input bias current, very low input current noise, and very low input voltage noise. As a result, these amplifiers are ideal choices for circuits with high impedance sensor applications.

Figure 52 shows the typical input noise of the LMP7701/LMP7702/LMP7704 as a function of source resistance where:

e_n denotes the input referred voltage noise

e_i is the voltage drop across source resistance due to input referred current noise or $e_i = R_S * i_n$

e_t shows the thermal noise of the source resistance

e_{ni} shows the total noise on the input.

Where:

$$e_{ni} = \sqrt{e_n^2 + e_i^2 + e_t^2}$$

The input current noise of the LMP7701/LMP7702/LMP7704 is so low that it will not become the dominant factor in the total noise unless source resistance exceeds 300 MΩ, which is an unrealistically high value.

As is evident in Figure 52, at lower R_S values, total noise is dominated by the amplifier's input voltage noise. Once R_S is larger than a few kilo-Ohms, then the dominant noise factor becomes the thermal noise of R_S. As mentioned before, the current noise will not be the dominant noise factor for any practical application.

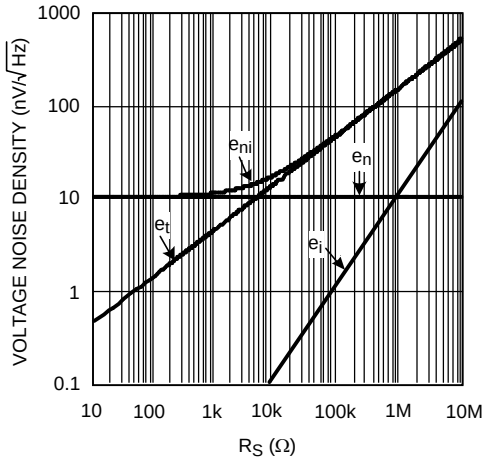


Figure 52. Total Input Noise

HIGH IMPEDANCE SENSOR INTERFACE

Many sensors have high source impedances that may range up to 10 MΩ. The output signal of sensors often needs to be amplified or otherwise conditioned by means of an amplifier. The input bias current of this amplifier can load the sensor's output and cause a voltage drop across the source resistance as shown in Figure 53, where $V_{IN}^{+} = V_S - I_{BIAS}*R_S$

The last term, $I_{BIAS}*R_S$, shows the voltage drop across R_S. To prevent errors introduced to the system due to this voltage, an op amp with very low input bias current must be used with high impedance sensors. This is to keep the error contribution by $I_{BIAS}*R_S$ less than the input voltage noise of the amplifier, so that it will not become the dominant noise factor.

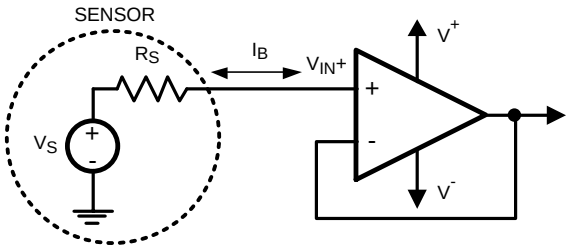


Figure 53. Noise Due to I_{BIAS}

pH electrodes are very high impedance sensors. As their name indicates, they are used to measure the pH of a solution. They usually do this by generating an output voltage which is proportional to the pH of the solution. pH electrodes are calibrated so that they have zero output for a neutral solution, pH = 7, and positive and negative voltages for acidic or alkaline solutions. This means that the output of a pH electrode is bipolar and has to be level shifted to be used in a single supply system. The rate of change of this voltage is usually shown in mV/pH and is different for different pH sensors. Temperature is also an important factor in a pH electrode reading. The output voltage of the senor will change with temperature.

Figure 54 shows a typical output voltage spectrum of a pH electrode. Note that the exact values of output voltage will be different for different sensors. In this example, the pH electrode has an output voltage of 59.15 mV/pH at 25°C.

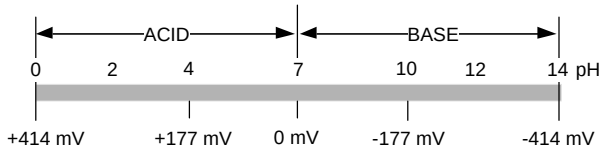


Figure 54. Output Voltage of a pH Electrode

The temperature dependence of a typical pH electrode is shown in Figure 55. As is evident, the output voltage changes with changes in temperature.

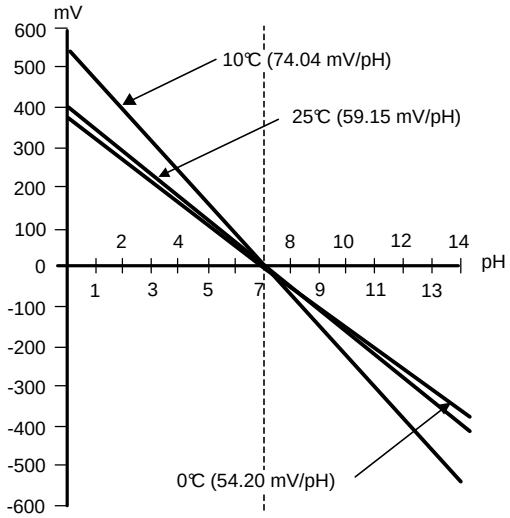


Figure 55. Temperature Dependence of a pH Electrode

The schematic shown in Figure 56 is a typical circuit which can be used for pH measurement. The LM35 is a precision integrated circuit temperature sensor. This sensor is differentiated from similar products because it has an output voltage linearly proportional to Celcius measurement, without the need to convert the temperature to Kelvin. The LM35 is used to measure the temperature of the solution and feeds this reading to the Analog to Digital Converter, ADC. This information is used by the ADC to calculate the temperature effects on the pH readings. The LM35 needs to have a resistor, R_T in Figure 56, to $-V^+$ in order to be able to read temperatures below 0°C. R_T is not needed if temperatures are not expected to go below zero.

The output of pH electrodes is usually large enough that it does not require much amplification; however, due to the very high impedance, the output of a pH electrode needs to be buffered before it can go to an ADC. Since most ADCs are operated on single supply, the output of the pH electrode also needs to be level shifted. Amplifier A1 buffers the output of the pH electrode with a moderate gain of +2, while A2 provides the level shifting. V_{OUT} at the output of A2 is given by: $V_{OUT} = -2V_{pH} + 1.024V$.

The LM4140A is a precision, low noise, voltage reference used to provide the level shift needed. The ADC used in this application is the ADC12032 which is a 12-bit, 2 channel converter with multiplexers on the inputs and a serial output. The 12-bit ADC enables users to measure pH with an accuracy of 0.003 of a pH unit. Adequate power supply bypassing and grounding is extremely important for ADCs. Recommended bypass capacitors are shown in Figure 56. It is common to share power supplies between different components in a circuit. To minimize the effects of power supply ripples caused by other components, the op amps need to have bypass capacitors on the supply pins. Using the same value capacitors as those used with the ADC are ideal. The combination of these three values of capacitors ensures that AC noise present on the power supply line is grounded and does not interfere with the amplifiers' signal.

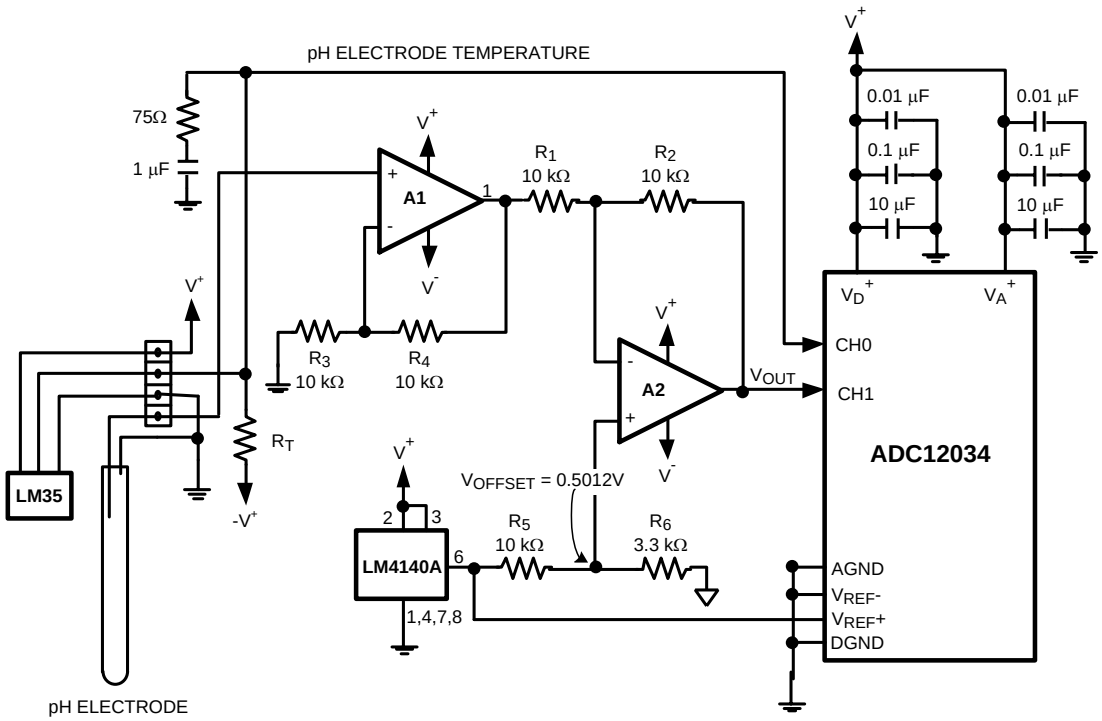


Figure 56. pH Measurement Circuit

REVISION HISTORY

Changes from Revision G (March 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	23

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP7701MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMP77 01MA	Samples
LMP7701MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMP77 01MA	Samples
LMP7701MF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	AC2A	
LMP7701MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AC2A	Samples
LMP7701MFX	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	AC2A	
LMP7701MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AC2A	Samples
LMP7702MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMP77 02MA	Samples
LMP7702MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMP77 02MA	Samples
LMP7702MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	AA3A	
LMP7702MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AA3A	Samples
LMP7702MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AA3A	Samples
LMP7704MA/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMP7704 MA	Samples
LMP7704MAX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMP7704 MA	Samples
LMP7704MT	NRND	TSSOP	PW	14	94	TBD	Call TI	Call TI	-40 to 125	LMP77 04MT	
LMP7704MT/NOPB	ACTIVE	TSSOP	PW	14	94	Pb-Free (RoHS)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP77 04MT	Samples
LMP7704MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Pb-Free (RoHS)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP77 04MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

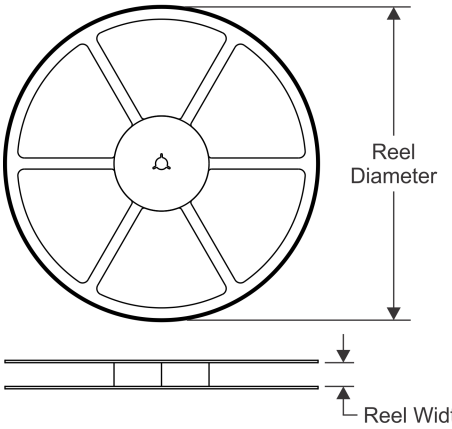
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

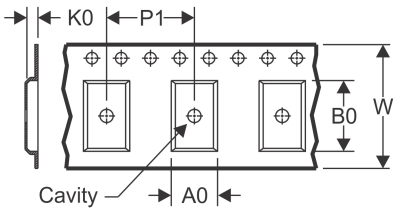
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

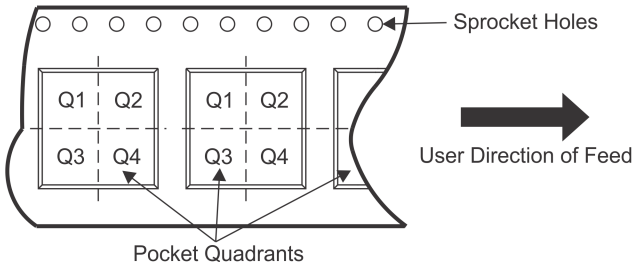


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

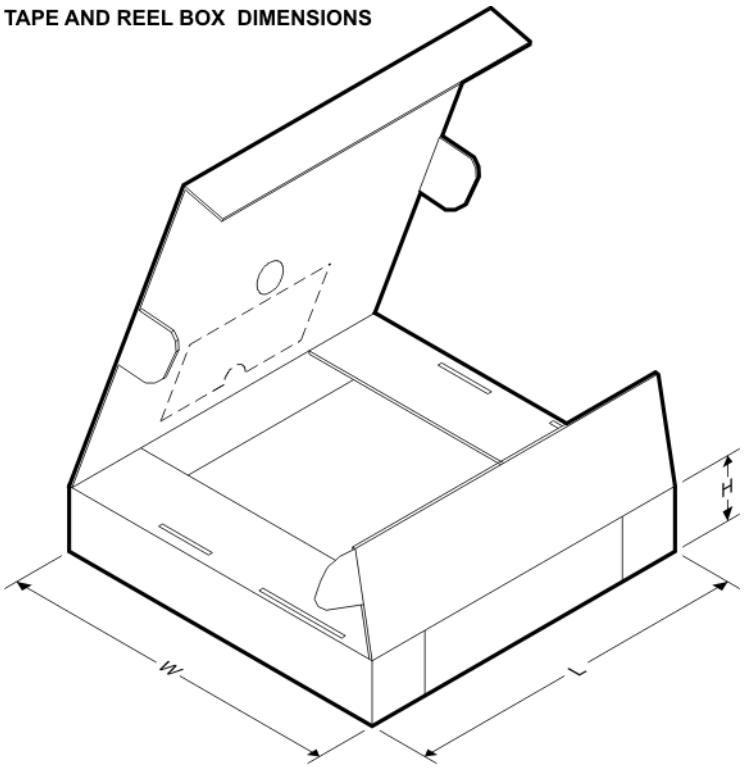
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP7701MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP7701MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7701MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7701MFX	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7701MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7702MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP7702MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7702MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7702MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7704MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMP7704MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1

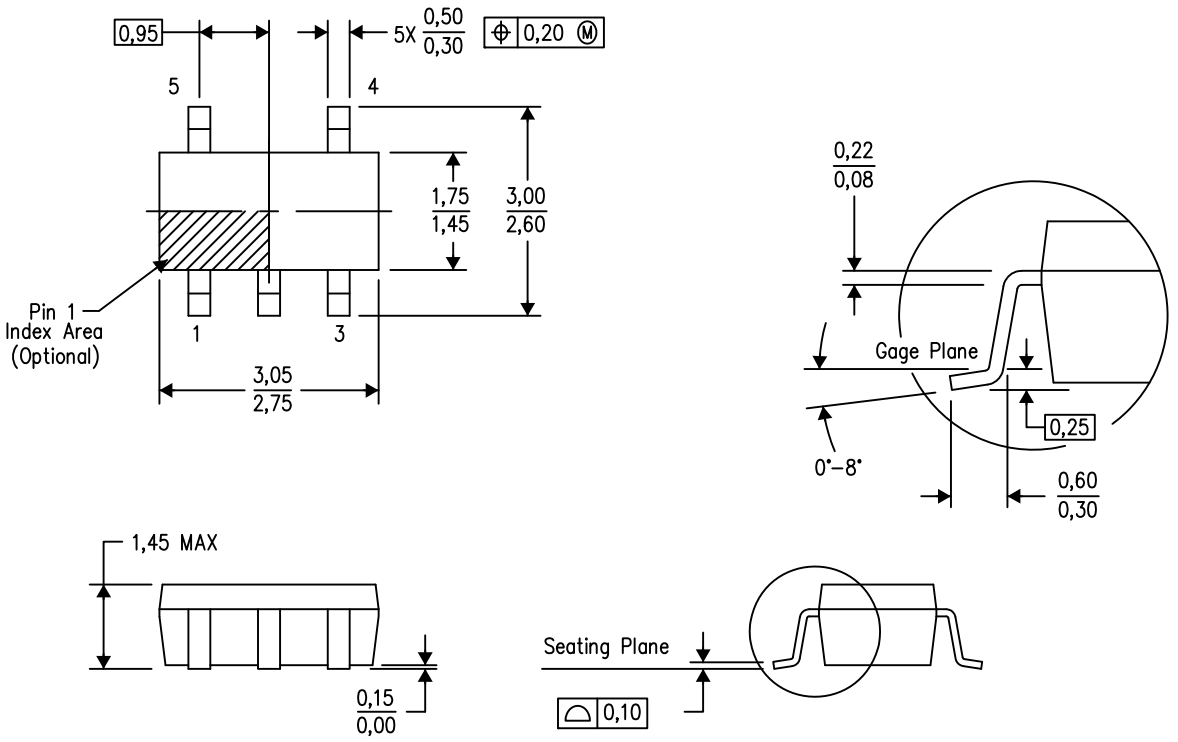
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP7701MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP7701MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMP7701MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMP7701MFX	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMP7701MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMP7702MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP7702MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP7702MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP7702MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMP7704MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMP7704MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

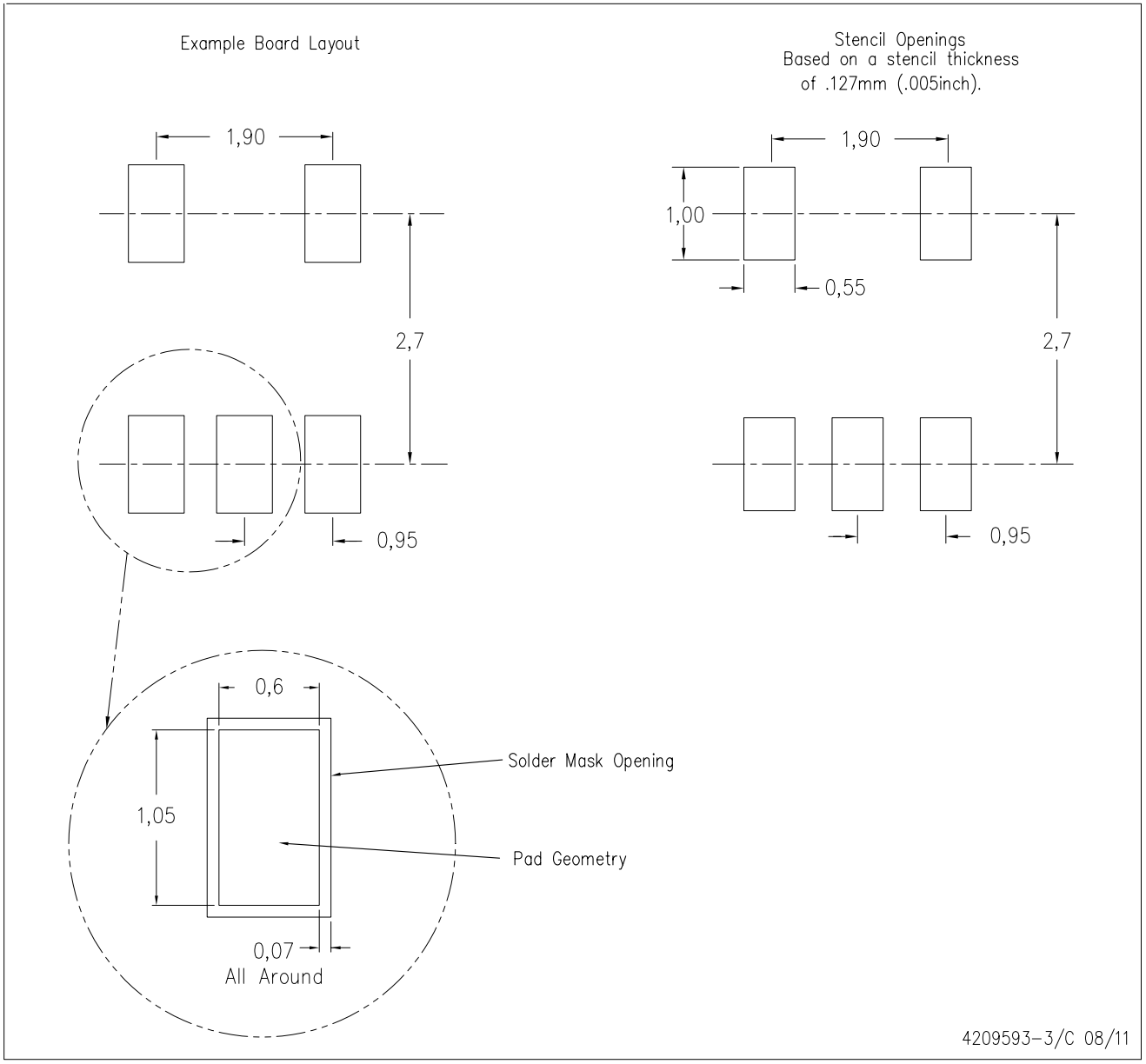
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/M 11/14

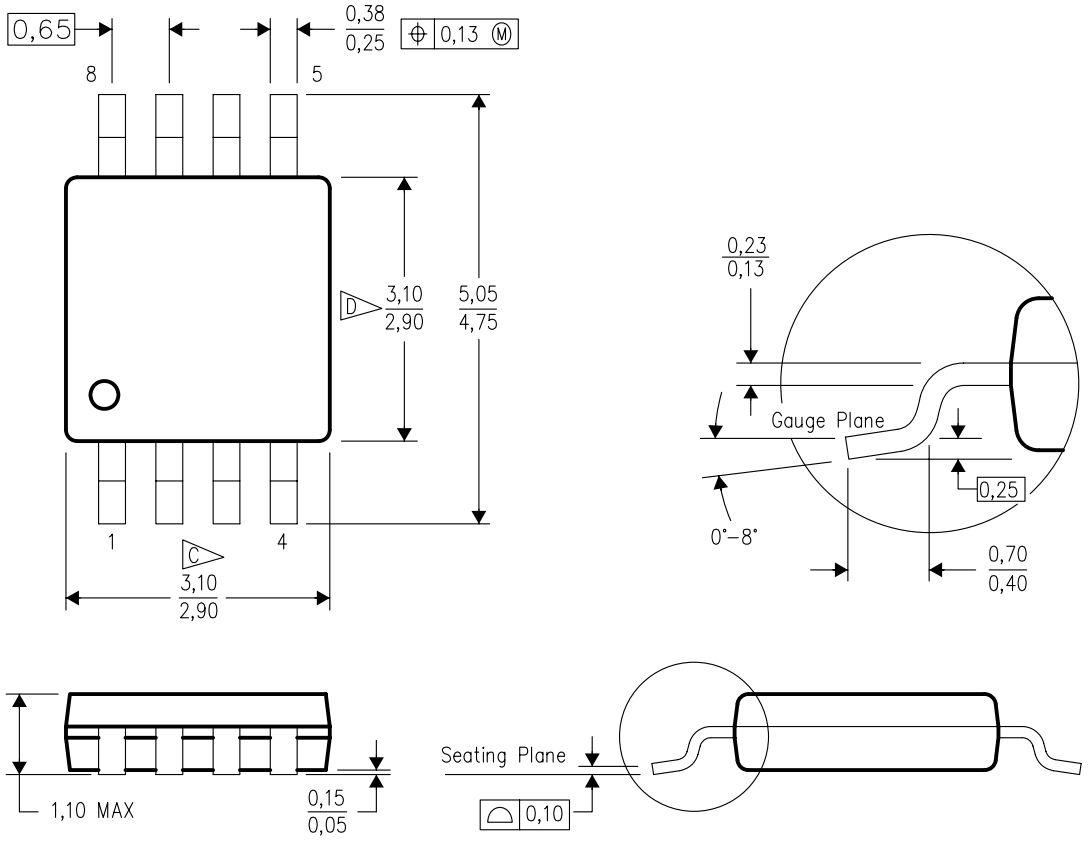
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

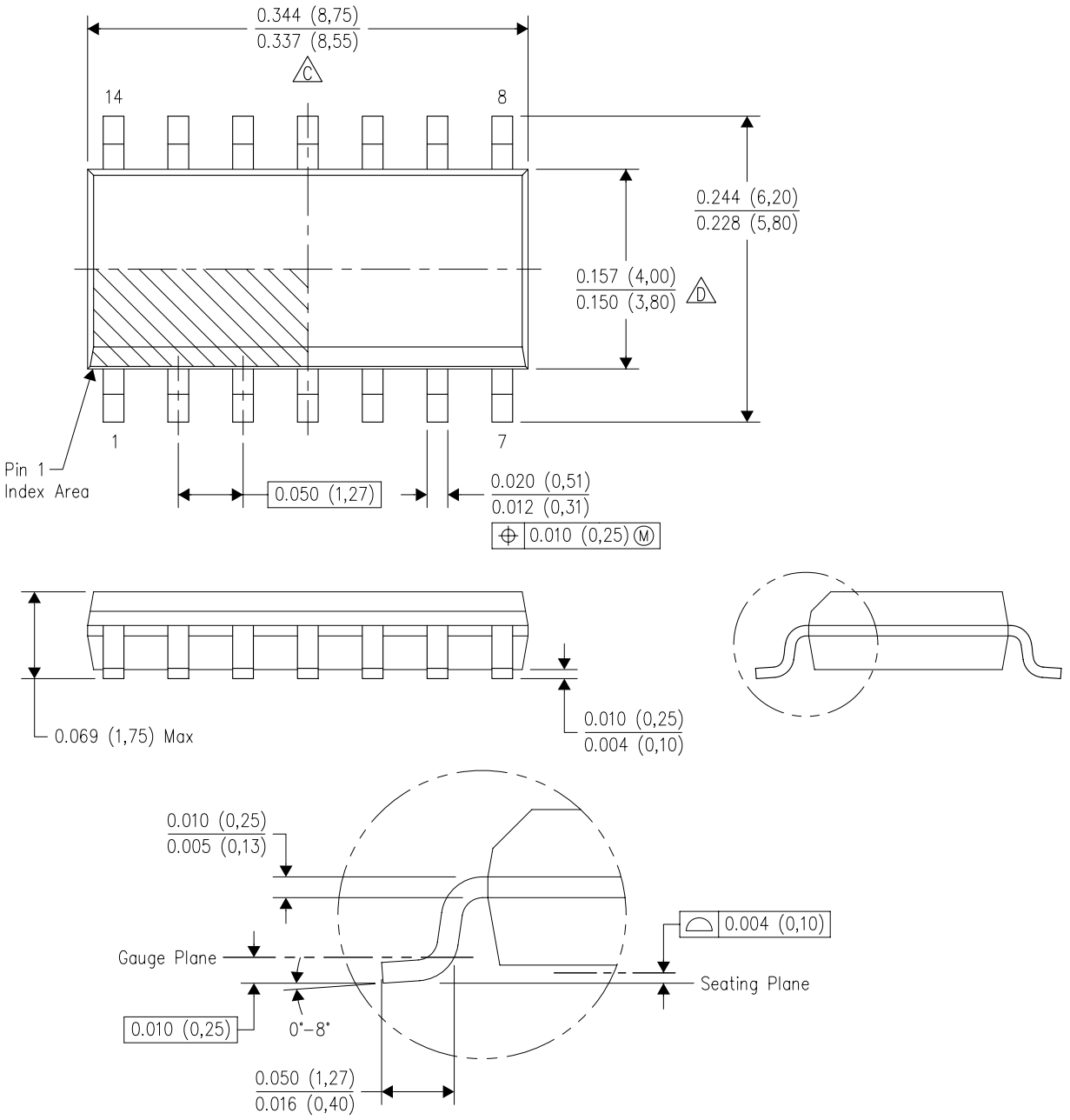
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

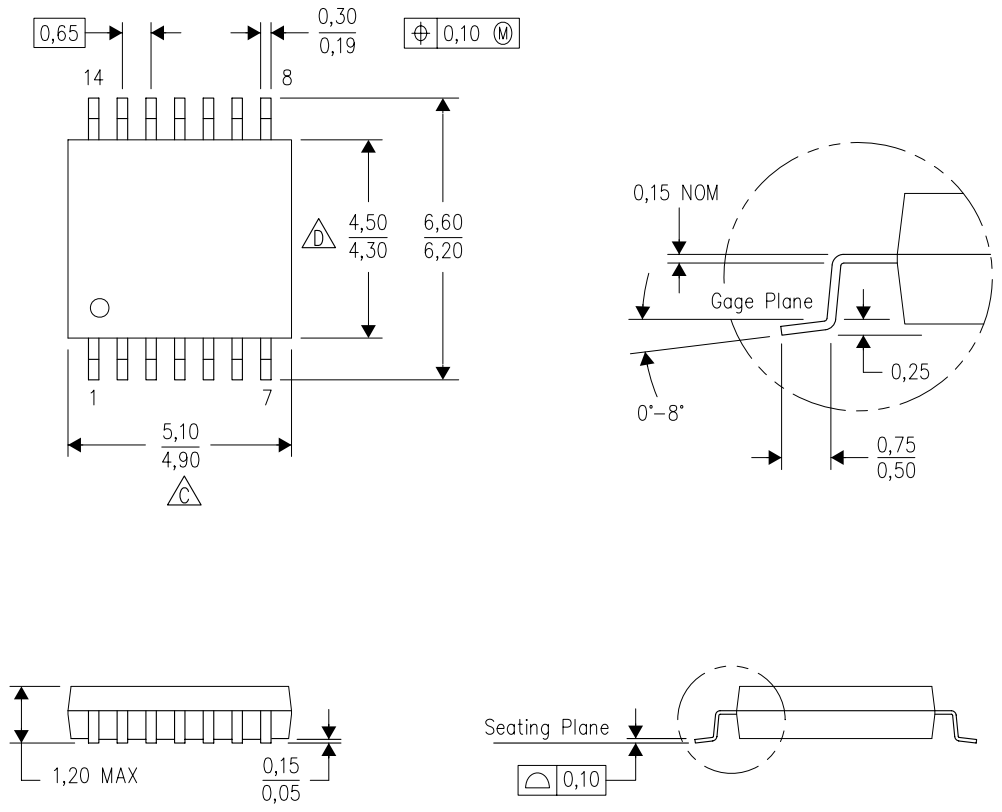
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

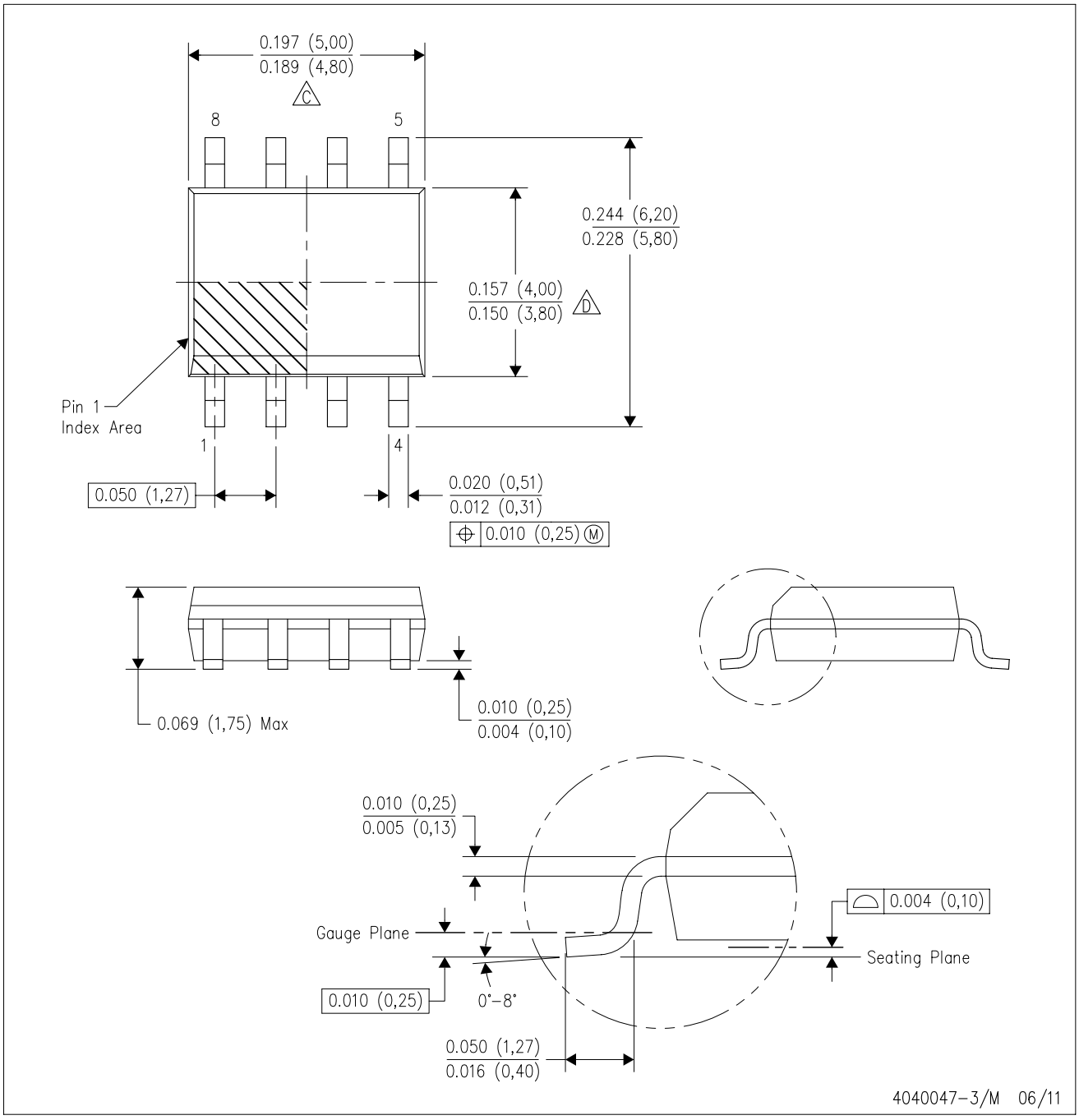
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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