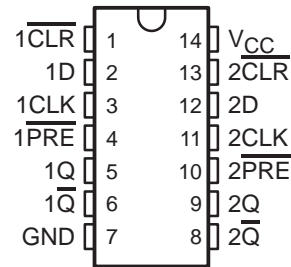- **2-V to 6-V V_{CC} Operation**
- **Inputs Accept Voltages to 6 V**
- **Max t_{pd} of 10 ns at 5 V**
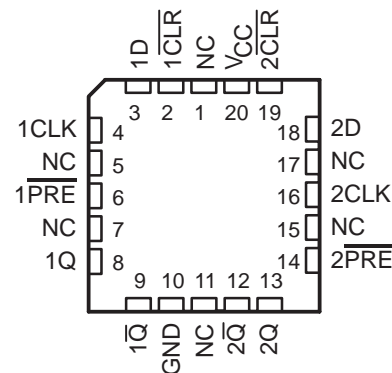
description/ordering information

The 'AC74 devices are dual positive-edge-triggered D-type flip-flops.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) input sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at D can be changed without affecting the levels at the outputs.

SN54AC74 . . . J OR W PACKAGE
SN74AC74 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)

```
1CLR  [ 1      14 ]  V_CC
  1D  [ 2      13 ]  2CLR
1CLK  [ 3      12 ]  2D
1PRE  [ 4      11 ]  2CLK
  1Q  [ 5      10 ]  2PRE
  1Q  [ 6       9 ]  2Q
 GND  [ 7       8 ]  2Q
```

SN54AC74 . . . FK PACKAGE
(TOP VIEW)

```
          1D  1CLR  NC  V_CC  2CLR
           3    2    1   20    19
1CLK  [ 4                        18 ]  2D
  NC  [ 5                        17 ]  NC
1PRE  [ 6                        16 ]  2CLK
  NC  [ 7                        15 ]  NC
  1Q  [ 8                        14 ]  2PRE
           9   10   11   12   13
          1Q  GND   NC   2Q   2Q
```

NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube	SN74AC74N	SN74AC74N
	SOIC – D	Tube	SN74AC74D	AC74
		Tape and reel	SN74AC74DR	
	SOP – NS	Tape and reel	SN74AC74NSR	AC74
	SSOP – DB	Tape and reel	SN74AC74DBR	AC74
	TSSOP – PW	Tube	SN74AC74PW	AC74
		Tape and reel	SN74AC74PWR	
−55°C to 125°C	CDIP – J	Tube	SNJ54AC74J	SNJ54AC74J
	CFP – W	Tube	SNJ54AC74W	SNJ54AC74W
	LCCC – FK	Tube	SNJ54AC74FK	SNJ54AC74FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is unstable; that is, it does not persist when either $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

logic diagram, each flip-flop (positive logic)

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . ±200 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . 86°C/W
DB package . . . . 96°C/W
N package . . . . 80°C/W
NS package . . . . 76°C/W
PW package . . . . 113°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
        2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54AC74		SN74AC74		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	6	2	6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1		2.1		V
		V_{CC} = 4.5 V	3.15		3.15		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 3 V		0.9		0.9	V
		V_{CC} = 4.5 V		1.35		1.35	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V		−12		−12	mA
		V_{CC} = 4.5 V		−24		−24	
		V_{CC} = 5.5 V		−24		−24	
I_{OL}	Low-level output current	V_{CC} = 3 V		12		12	mA
		V_{CC} = 4.5 V		24		24	
		V_{CC} = 5.5 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			8		8	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report,
        Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

TEXAS
INSTRUMENTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25°C$			SN54AC74		SN74AC74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		$I_{OH} = -50$ µA	3 V	2.9	4.49		2.9		2.9		V
			4.5 V	4.4	5.49		4.4		4.4		
			5.5 V	5.4	5.49		5.4		5.4		
		$I_{OH} = -12$ mA	3 V	2.56			2.4		2.46		
		$I_{OH} = -24$ mA	4.5 V	3.86			3.7		3.76		
			5.5 V	4.86			4.7		4.76		
		$I_{OH} = -50$ mA†	5.5 V				3.85				
		$I_{OH} = -75$ mA†	5.5 V						3.85		
V_{OL}		$I_{OL} = 50$ µA	3 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			5.5 V		0.001	0.1		0.1		0.1	
		$I_{OL} = 12$ mA	3 V			0.36		0.5		0.44	
		$I_{OL} = 24$ mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		$I_{OL} = 50$ mA†	5.5 V					1.65			
		$I_{OL} = 75$ mA†	5.5 V							1.65	
I_I	Data pins	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
	Control pins					±0.1		±1		±1	
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		40		20	µA
C_i		$V_I = V_{CC}$ or GND	5 V		3						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

timing requirements over recommended operating free-air temperature range,
$V_{CC} = 3.3$ V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

			$T_A = 25°C$		SN54AC74		SN74AC74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			100		70		95	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	5.5		8		7		ns
		CLK	5.5		8		7		
t_{su}	Setup time, data before CLK↑	Data	4		5		4.5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	0		0.5		0		
t_h	Hold time, data after CLK↑		0.5		0.5		0.5		ns

timing requirements over recommended operating free-air temperature range,
V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54AC74		SN74AC74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			140		95		125	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4.5		5.5		5		ns
		CLK	4.5		5.5		5		
t_{su}	Setup time, data before CLK↑	Data	3		4		3		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	0		0.5		0		
t_h	Hold time, data after CLK↑		0.5		0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54AC74		SN74AC74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	125		70		95		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3.5	8	12	1	13	2.5	13	ns
t_{PHL}			4	10.5	12	1	14	3.5	13.5	
t_{PLH}	CLK	Q or $\overline{Q}$	4.5	8	13.5	1	17.5	4	16	ns
t_{PHL}			3.5	8	14	1	13.5	3.5	14.5	

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54AC74		SN74AC74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			140	160		95		125		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2.5	6	9	1	9.5	2	10	ns
t_{PHL}			3	8	9.5	1	10.5	2.5	10.5	
t_{PLH}	CLK	Q or $\overline{Q}$	3.5	6	10	1	12	3	10.5	ns
t_{PHL}			2.5	6	10	1	10	2.5	10.5	

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
C_{pd} Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	45	pF

PARAMETER MEASUREMENT INFORMATION
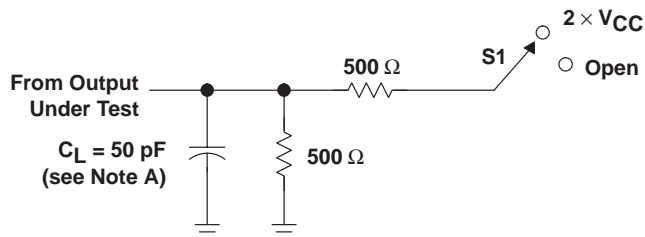
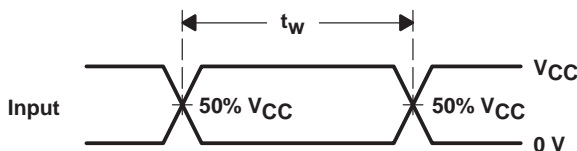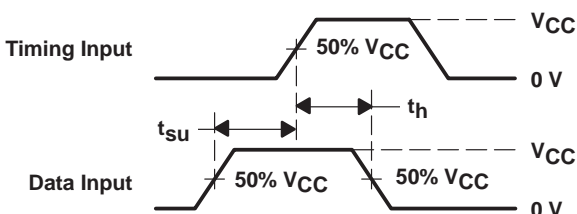| TEST	S1
t_{PLH}/t_{PHL}	Open

LOAD CIRCUIT
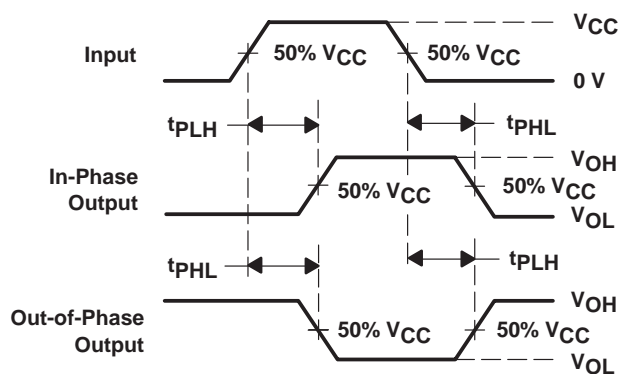
VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
       B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
       C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-88520012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-88520012A SNJ54AC 74FK	Samples
5962-8852001CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8852001CA SNJ54AC74J	Samples
5962-8852001DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8852001DA SNJ54AC74W	Samples
5962-8852001VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8852001VCA SNV54AC74J	Samples
5962-8852001VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8852001VDA SNV54AC74W	Samples
SN74AC74D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SN74AC74DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	-40 to 85		
SN74AC74DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SN74AC74DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SN74AC74DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SN74AC74DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SN74AC74DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SN74AC74DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SN74AC74N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC74N	Samples
SN74AC74NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC74N	Samples
SN74AC74NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AC74PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SN74AC74PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SN74AC74PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85		
SN74AC74PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SN74AC74PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SN74AC74PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SNJ54AC74FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-88520012A SNJ54AC 74FK	Samples
SNJ54AC74J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8852001CA SNJ54AC74J	Samples
SNJ54AC74W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8852001DA SNJ54AC74W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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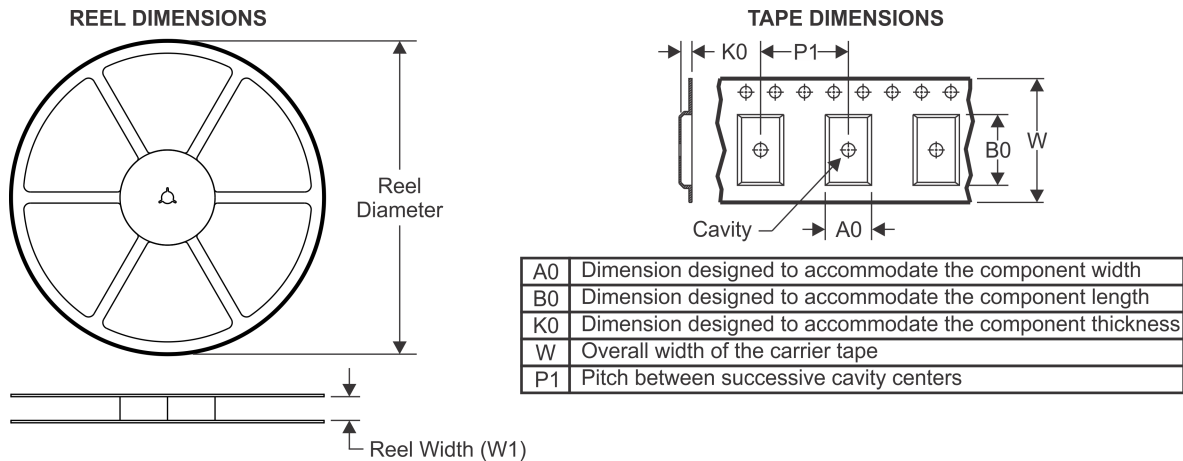
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AC74, SN54AC74-SP, SN74AC74 :

• Catalog: SN74AC74, SN54AC74

• Enhanced Product: SN74AC74-EP, SN74AC74-EP

• Military: SN54AC74

• Space: SN54AC74-SP

NOTE: Qualified Version Definitions:

     • Catalog - TI's standard catalog product

     • Enhanced Product - Supports Defense, Aerospace and Medical Applications

     • Military - QML certified for Military and Defense Applications

     • Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC74DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AC74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC74NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AC74PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC74DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74AC74DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74AC74DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74AC74NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74AC74PWR	TSSOP	PW	14	2000	367.0	367.0	35.0

DIM PINS ∗∗	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03
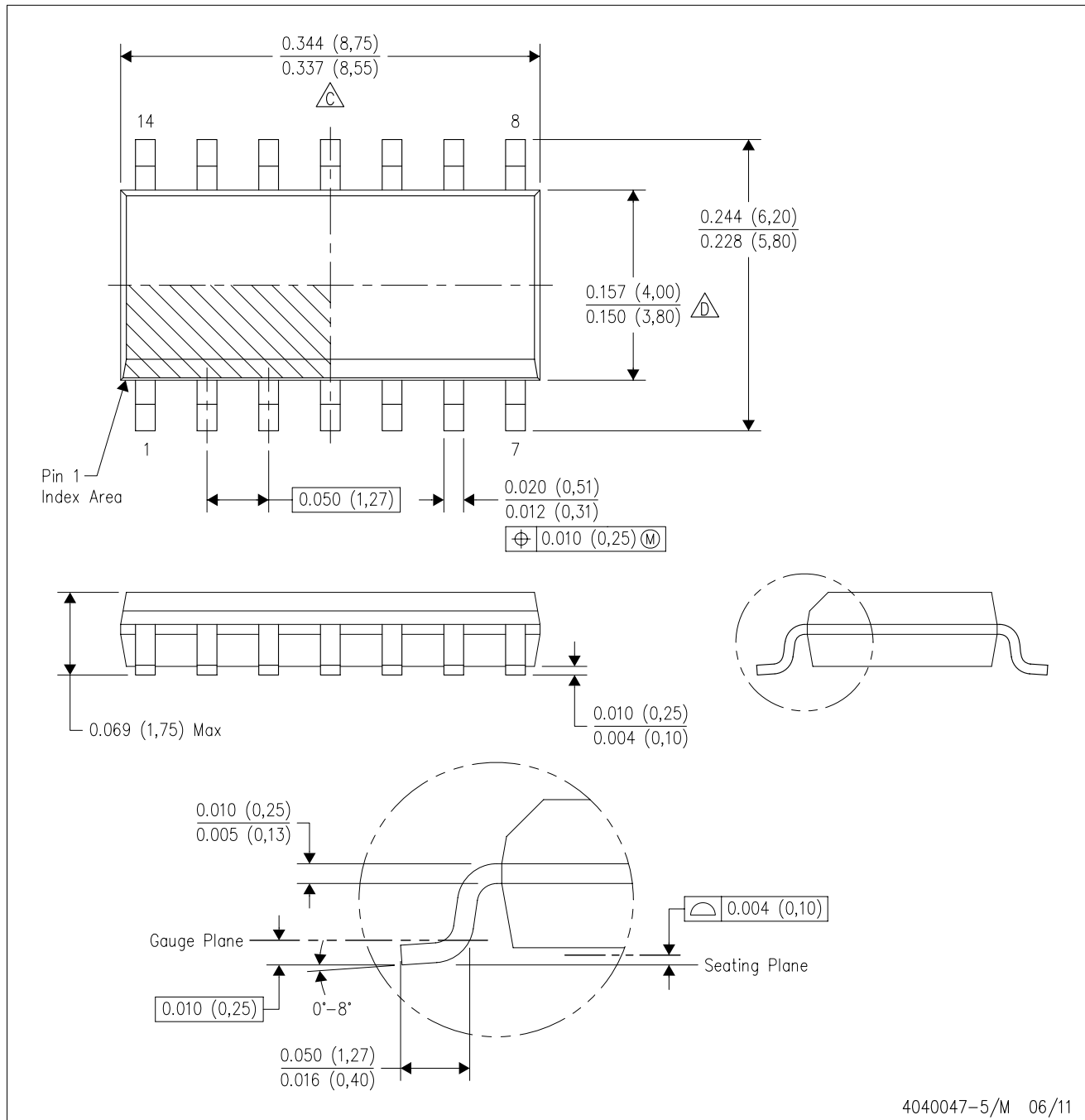
NOTES: A.   All linear dimensions are in inches (millimeters).
B.   This drawing is subject to change without notice.
C.   This package is hermetically sealed with a ceramic lid using glass frit.
D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E.   Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

W (R−GDFP−F14)   CERAMIC DUAL FLATPACK
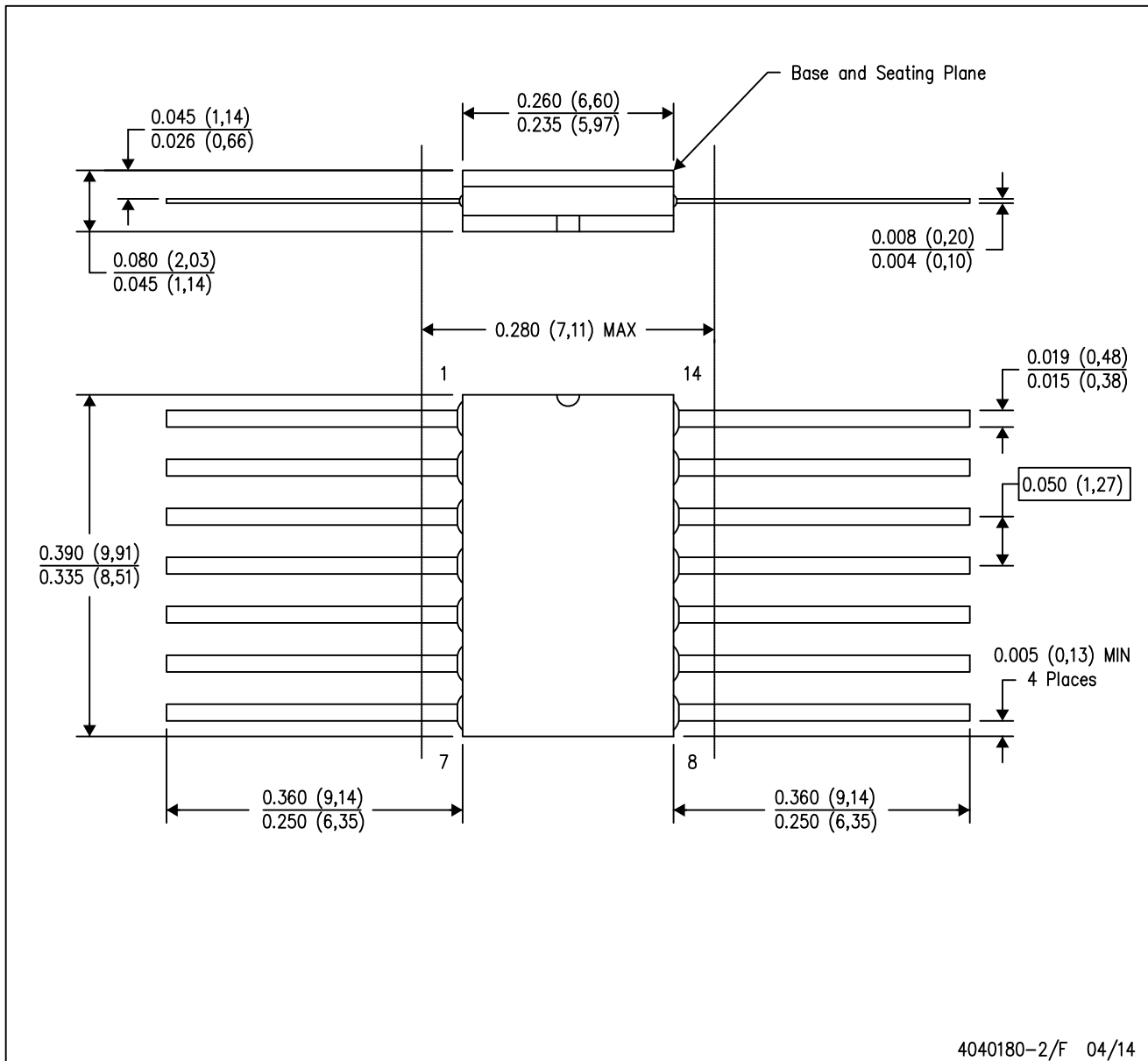
Base and Seating Plane

$\dfrac{0.045\ (1,14)}{0.026\ (0,66)}$

$\dfrac{0.260\ (6,60)}{0.235\ (5,97)}$

$\dfrac{0.080\ (2,03)}{0.045\ (1,14)}$

$\dfrac{0.008\ (0,20)}{0.004\ (0,10)}$

0.280 (7,11) MAX

$\dfrac{0.019\ (0,48)}{0.015\ (0,38)}$

1   14

0.050 (1,27)

$\dfrac{0.390\ (9,91)}{0.335\ (8,51)}$

0.005 (0,13) MIN
4 Places

7   8

$\dfrac{0.360\ (9,14)}{0.250\ (6,35)}$ $\dfrac{0.360\ (9,14)}{0.250\ (6,35)}$

4040180−2/F   04/14

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package can be hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only.
         E. Falls within MIL STD 1835 GDFP1−F14

TEXAS INSTRUMENTS
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FK (S−CQCC−N**)   LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

$\dfrac{0.020\ (0,51)}{0.010\ (0,25)}$

$\dfrac{0.020\ (0,51)}{0.010\ (0,25)}$

$\dfrac{0.080\ (2,03)}{0.064\ (1,63)}$

$\dfrac{0.055\ (1,40)}{0.045\ (1,14)}$

$\dfrac{0.045\ (1,14)}{0.035\ (0,89)}$

$\dfrac{0.028\ (0,71)}{0.022\ (0,54)}$

0.050 (1,27)

$\dfrac{0.045\ (1,14)}{0.035\ (0,89)}$

4040140/D 01/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a metal lid.
         D.   Falls within JEDEC MS−004

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INSTRUMENTS
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N (R–PDIP–T**)

16 PINS SHOWN

PLASTIC DUAL–IN–LINE PACKAGE

	PINS ** DIM	14	16	18	20
A	MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A	MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C	MS–001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14) D

0.045 (1,14)
0.030 (0,76) D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) M

14/18 Pin Only
20 Pin vendor option D

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
         D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0.344 (8,75)
0.337 (8,55)
Ⓒ

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)   Ⓓ
0.150 (3,80)

Pin 1
Index Area

1   7

0.050 (1,27)   0.020 (0,51)
                    0.012 (0,31)

⊕ | 0.010 (0,25) | Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

| 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−5/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
      Ⓒ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0.006 (0,15) each side.
      Ⓓ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AB.

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D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

12x1,27

14x0,55

12x1,27

14x1,50

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

Example
Solder Mask Opening
(See Note E)

1,55

0.07
All Around

4211283−3/E 08/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0,65   0,30
              0,19   ⊕ 0,10 Ⓜ

14   8

         ⚠D   4,50   6,60
              4,30   6,20

1   7

    5,10
    4,90
     ⚠C

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX   0,15
                  0,05

Seating Plane

▱ 0,10

4040064−3/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
      ⚠C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
      ⚠D.   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

PW (R−PDSO−G14)   PLASTIC SMALL OUTLINE
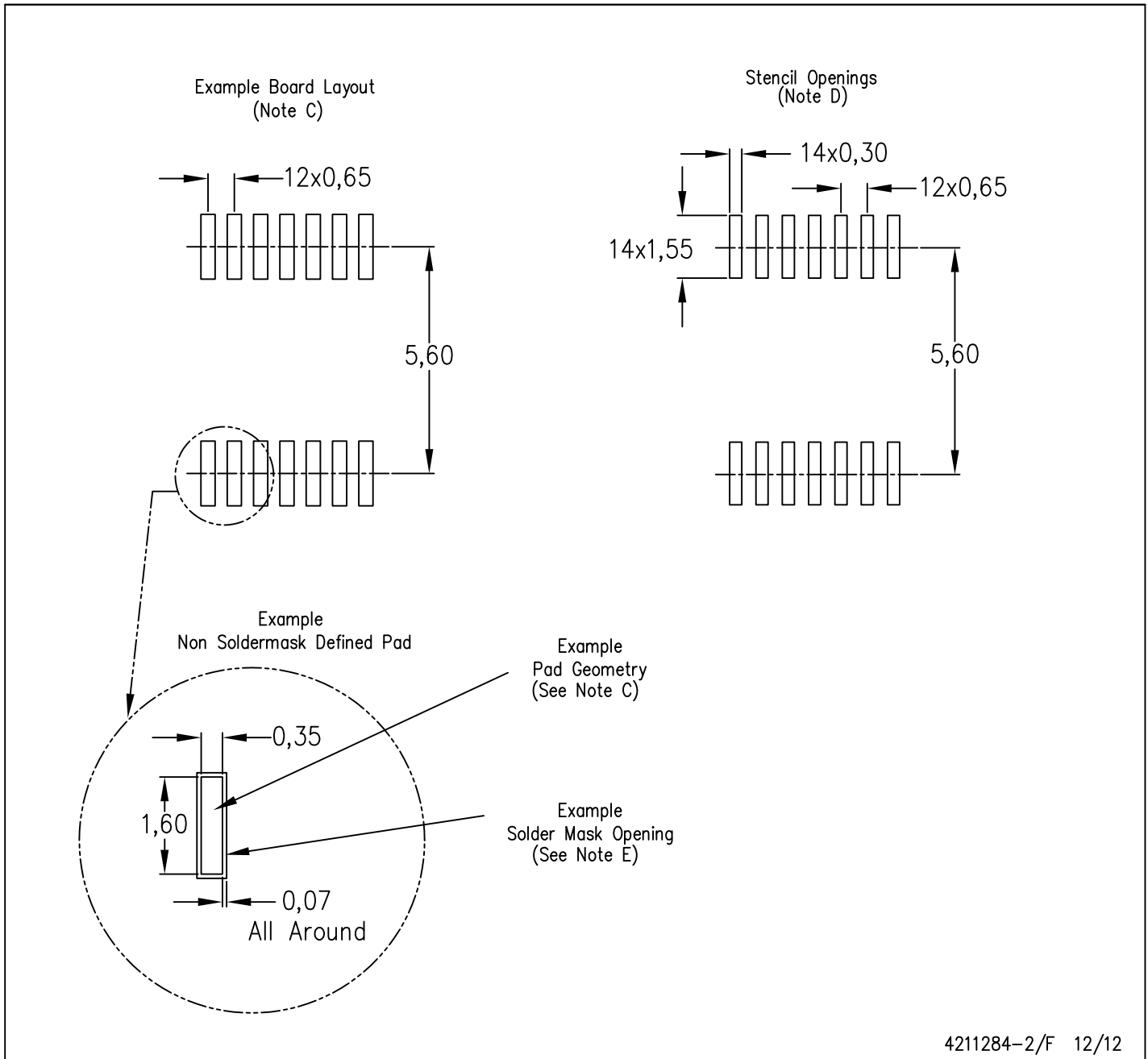
Example Board Layout
(Note C)

←12x0,65

5,60

Stencil Openings
(Note D)

←14x0,30

←12x0,65

14x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

←0,35

1,60

Example
Solder Mask Opening
(See Note E)

←0,07
All Around

4211284−2/F   12/12

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate designs.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
           B.   This drawing is subject to change without notice.
           C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

0,65

0,38
0,22   ⊕   0,15 Ⓜ

28   15

5,60
5,00   8,20
7,40

0,25
0,09

Gage Plane

0,25

0°−8°

0,95
0,55

1   14

A

2,00 MAX   0,05 MIN

Seating Plane

△ 0,10

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A.   All linear dimensions are in millimeters.
            B.   This drawing is subject to change without notice.
            C.   Body dimensions do not include mold flash or protrusion not to exceed 0,15.
            D.   Falls within JEDEC MO-150

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